Raptor Chip

Chip Databook

v1.30 | 2024-11-04

Document History

Version	Date	Authors	Description of Change
v1.00	2024-03-31	Neuchips	Initial release
v1.10	2024-08-02	Neuchips	Update design spec
v1.20	2024-09-09	Neuchips	Update power on sequence
v1.30	2024-11-04	Neuchips	Update power supply/budget

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1 Overview

Neuchips Raptor series AI chip emphasizes generative-AI and recommendation system acceleration and achieves high power efficiency. Raptor includes two ARC HS48 processors, an ARC EV72 DSP, PCIe Gen 5, LPDDR5, and an AI accelerator that supports matrix computation, vector computation, and efficient embedding table lookup.

1.1 Features

- Embedded ARC HS48 processors
  - CPU0 - quad core with MMU function
  - CPU1 - dual core
- Embedded ARC EV72 processor
  - Vector DSP
  - FPU
- PCIe Gen 5 x 8
- 16 LPDDR5-6400 controllers
- AI accelerator
  - 10 matrix engines (Dynamic MLP Engine, DME)
  - 2 vector engines (Feature Cross, FX)
  - Embedding engine
- Crypto engines
  - Hardware root of trust with processor, TRNG, and OTP storage
- 512KB shared memory
- QSPI Flash controller, I^{2}C, SPI, UART, GPIO

Applications

Generative-AI models such as

1. LLaMA
2. Mistral
3. Gemma
4. Phi

Deep leaning-based recommendation models such as

1. Deep Learning Recommendation Model (DLRM)
2. Wide & Deep Learning (WND)
3. Deep & Cross Networks (DCN)
4. Neural Collaborative Filtering (NCF)

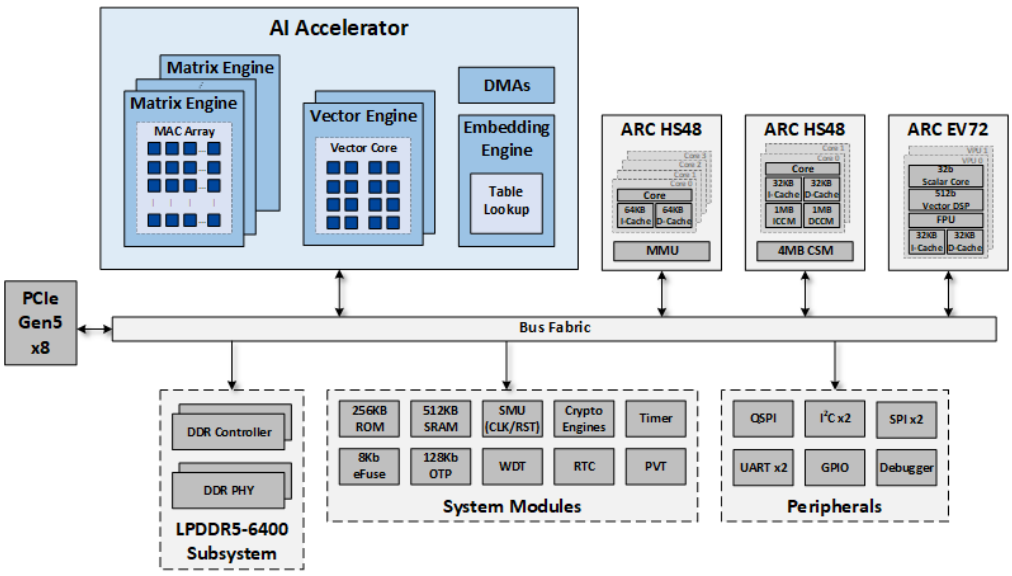


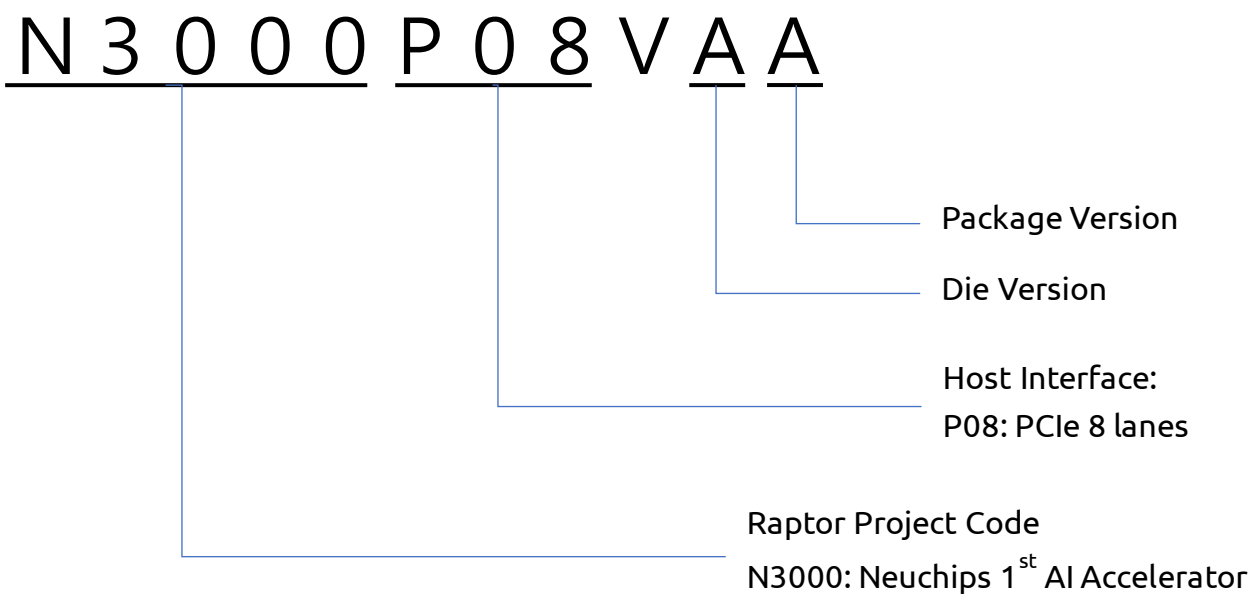
Figure 1 Functional Block Diagram

1.2 Part Number Ordering

The following tables list the parts that can be ordered.

Table 1 Part Numbers

Device	Part Number
Raptor	N3000P08VAA



2 Device Characteristics

2.1 Power Supply

The Table 2 shows the Raptor operating voltages.

Table 2 Operating Voltage

Power Supply	Voltage		Voltage Operating Limit (V)		
	Nominal	Tolerance (%)	Minimum	Nominal	Maximum
AVDD_PLL_DDR* AVDD_PLL1 AVDD_PLL2 VDD2_OTP2 VDDA_PVT VDDPST VQPS_EFUSE VQPS_EFUSE_REP	1.8	-10 ~ +10	1.62	1.8	1.98
CH*_VAA_VDD2H0 CH*_VAA_VDD2H1	1.8	-7 ~ +10	1.674	1.8	1.98
EP01_VPH*	1.2	-7 ~ +10	1.116	1.2	1.32
EP23_VPH*	1.8		1.674	1.8	1.98
CH*_VDD2H	1.08	-6.5 ~ +3.7	1.01	1.08	1.15
EP01_VDDL EP23_VDDL	0.9	-5 ~ +5	0.855	0.9	0.945
CH*_VDD	0.75	-5 ~ +5	0.7125	0.78	0.7875
DVDD_PLL_DDR**	0.82	-5 ~ +5	0.78	0.82	0.86
VDD	0.82	-5 ~ +5	0.78	0.82	0.86
VDD_MAC	0.75	-5 ~ +10	0.7125	0.69	0.825
CH*_VDDQ	0.5	-6 ~ +14	0.47	0.5	0.57

*: It can be supplied by 1.2V or 1.8V.

**: 1/2/3/4 for LPDDR Channel

2.2 DC Characteristic

Table 3 DC Characteristics

Parameter	Minimum	Nominal	Maximum	Units
V_{IL} Input Low Voltage	-0.3	-	0.35*VDDPST	V
V_{IH} Input High Voltage	0.65*VDDPST	-	VDDPST+0.3	V

V_{OL} Output Low Voltage	-	-	0.45	V
V_{OH} Output High Voltage	VDDPST-0.45	-	-	V
R_{PU} Pull-up Resistor	20	29	47	kΩ
R_{PD} Pull-down Resistor	19	27	44	kΩ

Except for LPDDR and PCIe, the DC characteristics of all signal pads are shown in table.

2.3 Power Budget

The Table 4 shows the Raptor operating power budget.

Table 4 Operating Power Budget

Power Supply	Current (A)
VDD	25
VDD_MAC	50
CH*_VDD	17
VCC1V05	6
VCC0V5	2.5
VCC1V8_1	2
VCC1V2	0.6
VCC0V9	3.0
VCC1V8_2	0.1

2.4 Package Thermal Characteristics

The Table 5 shows the Raptor package thermal characteristics. Conditions that exceed the operating limits can cause the device to function incorrectly.

Table 5 Package Thermal Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
T_J	Junction temperature	0	-	75	°C
T_A	Operating free air	0	-	50	°C
Θ_{JC}	Theta junction to case	-	0.06	-	°C/W
Θ_{JB}	Theta junction to board	-	0.21	-	°C/W

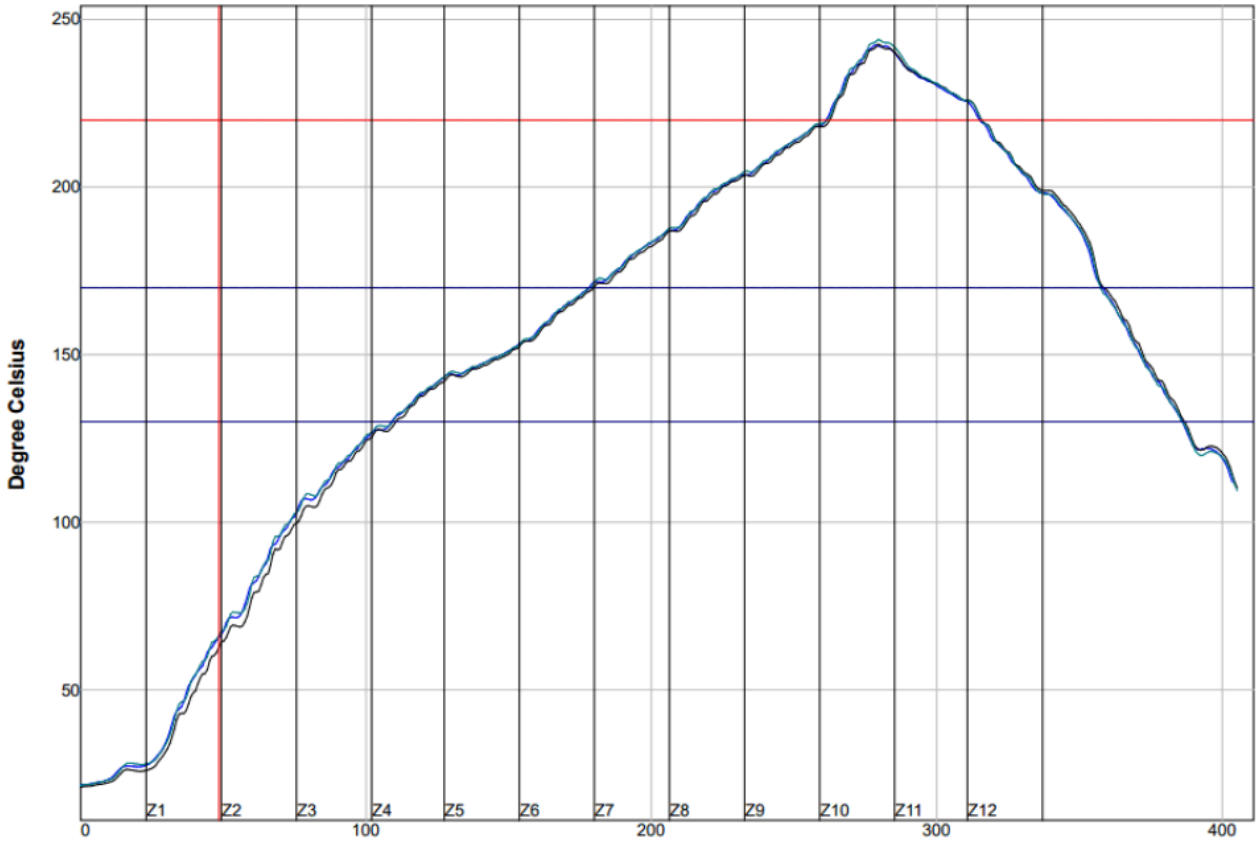
2.5 Heat Sink

Do not stress the Raptor component during attachment of the heat sink.

- During heat sink attachment, fully support the PCB under the component to prevent bowing and flexing of the PCB.

- Apply the force perpendicular to the component.
- Evenly distribute the pressure on the top side of the component.
- The maximum loading force is 140 psi.

2.6 SMT Reflow



	Preheat 130-170°C	Reflow Time /220°C	Peak Temp	Slope 1 (170-245°C)	Slope 2 (225-215°C)
VP 3	68.94	53.65	242.50	0.72	-1.34
VP 5	69.24	53.09	242.64	0.72	-1.41
VP 7	68.84	53.90	244.05	0.74	-1.46
Delta	0.40	0.81	1.55	0.02	0.12

Figure 2 SMT reflow profile

3 Pin Configurations

3.1 Ball Assignments

The Whole Picture

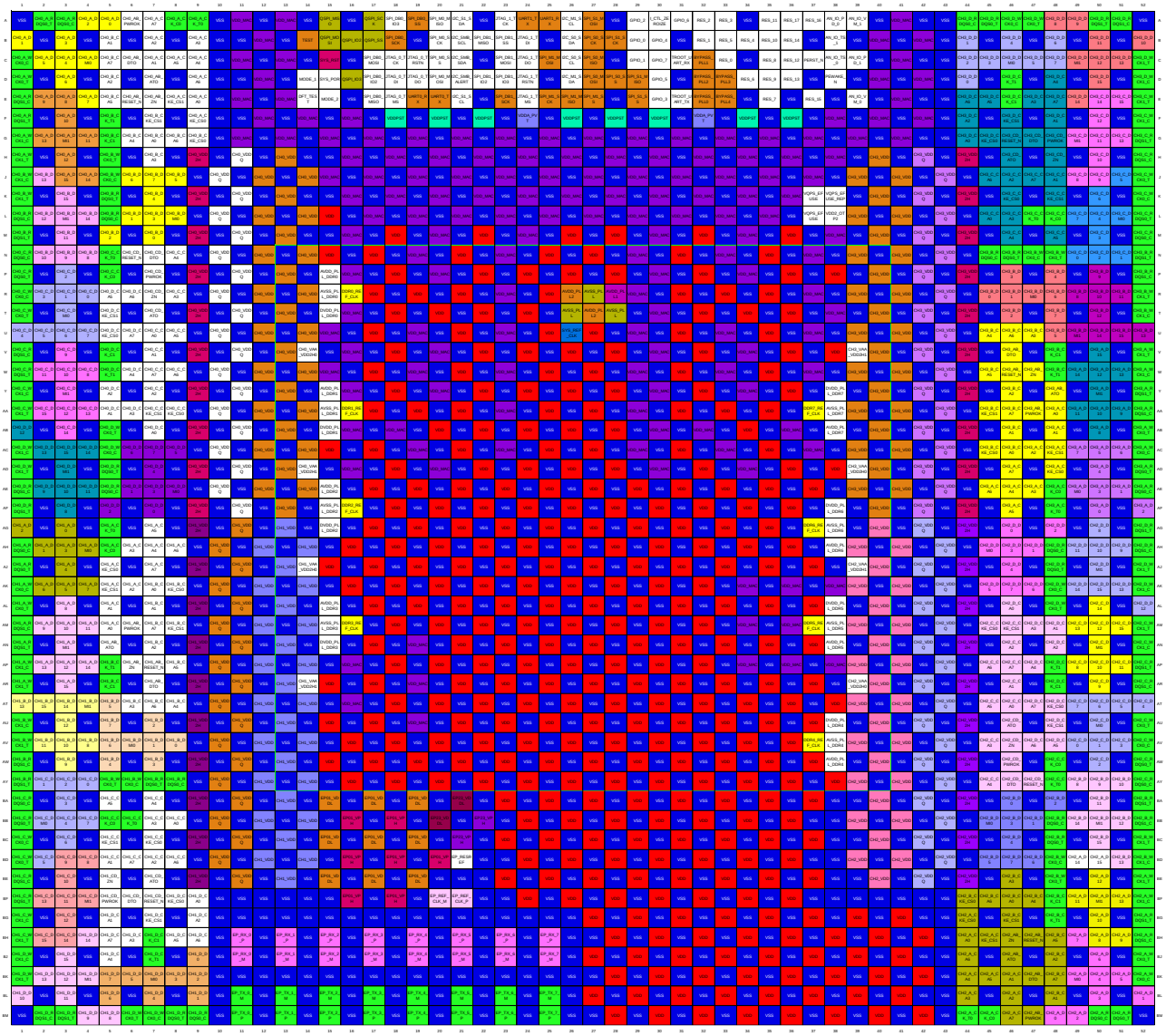


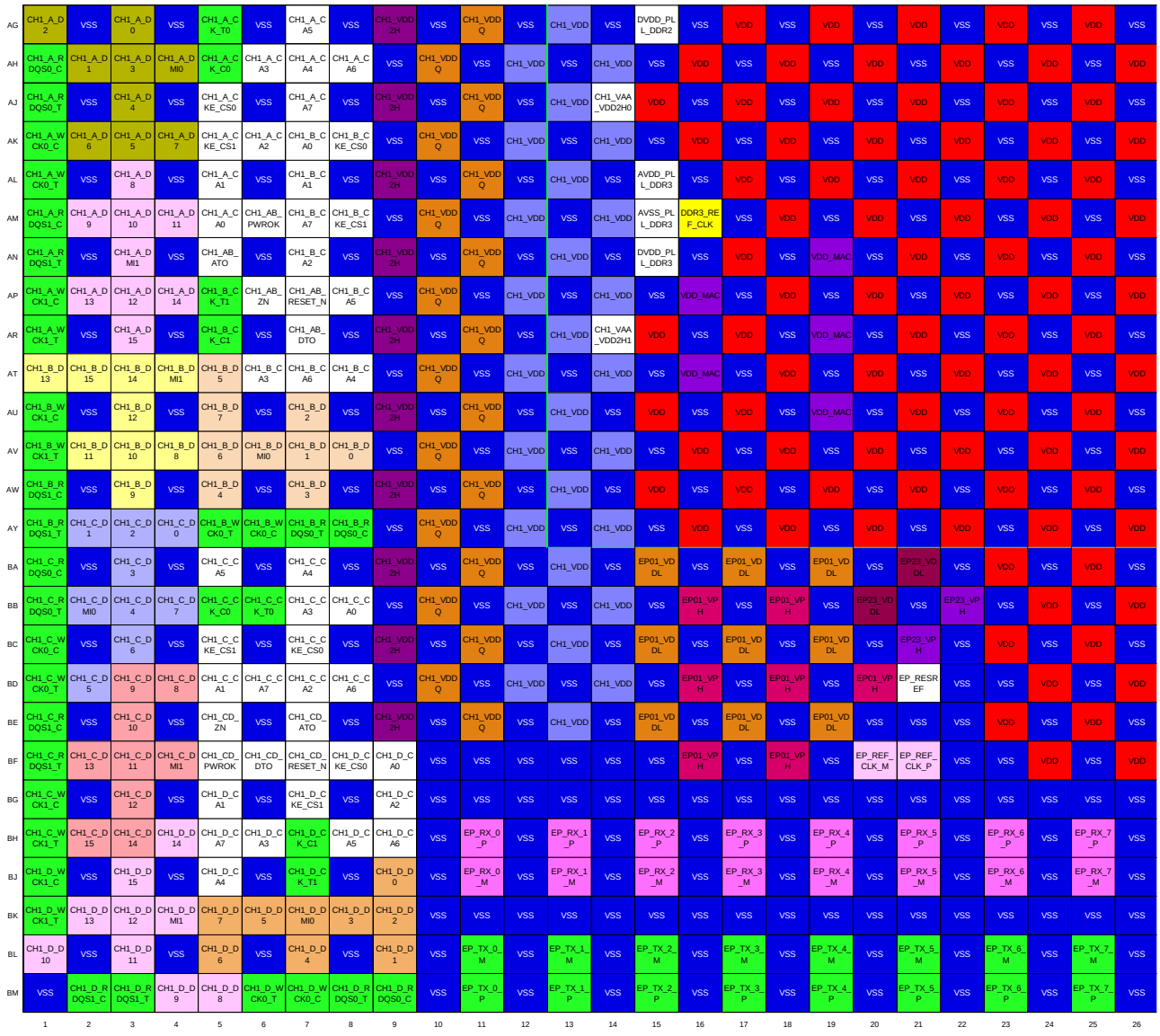
Figure 3 2704-Ball HFCBGA Ball Map

Top-Left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	CH0_A_RDQS0_T	CH0_A_RDQS0_C	CH0_A_D2	CH0_A_D0	CH0_AB_PWROK	CH0_A_CA7	CH0_A_CK_C0	CH0_A_CK_T0	VSS	VDD_MAC	VSS	VDD_MAC	VSS	QSPI_MISO	VSS	QSPI_SCK	SPI_DB0_IO3	SPI_DB0_SS	SPI_M0_MISO	I2C_S1_SDA	VSS	JTAG_1_TCK	UART1_TX	UART1_RX	I2C_M1_SCL
B	CH0_A_D1	VSS	CH0_A_D3	VSS	CH0_B_CA1	VSS	CH0_A_CA2	VSS	CH0_A_CA3	VSS	VSS	VDD_MAC	VSS	TEST	QSPI_MOSI	QSPI_IO2	QSPI_SS	SPI_DB0_SCK	VSS	SPI_M0_SCK	I2C_SMB_SCL	SPI_DB1_MISO	SPI_DB1_SS	JTAG_1_TDI	VSS	I2C_S0_SDA
C	CH0_A_WCK0_C	CH0_A_D5	CH0_A_D4	CH0_A_DMI0	CH0_B_CA7	CH0_AB_DTO	CH0_A_CA1	CH0_A_CA5	CH0_A_CA4	VSS	VDD_MAC	VSS	VDD_MAC	VSS	SYS_RST	VSS	SPI_DB0_MOSI	JTAG_0_TCK	JTAG_0_TRSTN	SPI_M0_SS	I2C_SMB_SDA	VSS	SPI_DB1_MOSI	JTAG_1_TDO	SPI_M1_MOSI	I2C_S0_SCL
D	CH0_A_WCK0_T	VSS	CH0_A_D6	VSS	CH0_B_CA2	VSS	CH0_AB_ATO	VSS	CH0_A_CA6	VSS	VSS	VDD_MAC	VSS	MODE_1	SYS_POR	QSPI_IO3	SPI_DB0_IO2	JTAG_0_TDI	JTAG_0_TDO	SPI_M0_MOSI	I2C_SMB_ALERT	SPI_DB1_IO2	SPI_DB1_IO3	JTAG_1_TRSTN	VSS	I2C_M1_SDA
E	CH0_A_RDQS1_C	CH0_A_D9	CH0_A_D8	CH0_A_D7	CH0_B_CA5	CH0_AB_RESET_N	CH0_AB_ZN	CH0_A_CKE_CS1	CH0_A_CA0	VSS	VDD_MAC	VSS	VDD_MAC	DFT_TEST	MODE_2	VSS	SPI_DB0_MISO	JTAG_0_TMS	UART0_RX	UART0_TX	I2C_S1_SCL	VSS	SPI_DB1_SCK	JTAG_1_TMS	SPI_M1_SCK	SPI_M1_MISO
F	CH0_A_RDQS1_T	VSS	CH0_A_D10	VSS	CH0_B_CK_T1	VSS	CH0_B_CKE_CS1	VSS	CH0_A_CKE_CS0	VSS	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDDPST	VSS	VDDPST	VSS	VDDPST	VSS	VDDA_PVT	VSS	VDDPST
G	CH0_A_WCK1_C	CH0_A_D13	CH0_A_DMI1	CH0_A_D11	CH0_B_CK_C1	CH0_B_CA4	CH0_B_CA0	CH0_B_CA6	CH0_B_CKE_CS0	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS
H	CH0_A_WCK1_T	VSS	CH0_A_D12	VSS	CH0_B_WCK0_T	VSS	CH0_B_CA3	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC
J	CH0_B_WCK1_C	CH0_B_D13	CH0_A_D15	CH0_A_D14	CH0_B_WCK0_C	CH0_B_D6	CH0_B_D7	CH0_B_D5	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS
K	CH0_B_WCK1_T	VSS	CH0_B_D15	VSS	CH0_B_RDQS0_T	VSS	CH0_B_D4	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC
L	CH0_B_RDQS1_C	CH0_B_D12	CH0_B_DMI1	CH0_B_D14	CH0_B_RDQS0_C	CH0_B_D1	CH0_B_D3	CH0_B_DMI0	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	VDD	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS
M	CH0_B_RDQS1_T	VSS	CH0_B_D11	VSS	CH0_B_D2	VSS	CH0_B_D0	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD
N	CH0_C_RDQS0_C	CH0_B_D10	CH0_B_D9	CH0_B_D8	CH0_C_CK_T0	CH0_CD_RESET_N	CH0_CD_DTO	CH0_C_CA4	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	VDD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS
P	CH0_C_RDQS0_T	VSS	CH0_C_D2	VSS	CH0_C_CK_C0	VSS	CH0_CD_PWROK	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	AVDD_PLL_DDR0	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD
R	CH0_C_WCK0_C	CH0_C_D3	CH0_C_D1	CH0_C_D0	CH0_D_CA5	CH0_D_CA6	CH0_CD_ZN	CH0_C_CA3	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	AVSS_PLL_DDR0	DDR0_REF_CLK	VDD	VSS	VDD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	AVDD_PLL2
T	CH0_C_WCK0_T	VSS	CH0_C_DMI0	VSS	CH0_D_CKE_CS1	VSS	CH0_CD_ATO	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	DVDD_PLL_DDR0	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	AVSS_PLL
U	CH0_C_D4	CH0_C_D5	CH0_C_D6	CH0_C_D7	CH0_D_CKE_CS0	CH0_D_CA7	CH0_C_CA0	CH0_C_CA5	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	SYS_REF_CLK
V	CH0_C_RDQS1_C	VSS	CH0_C_D9	VSS	CH0_D_CK_C1	VSS	CH0_C_CA1	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	CH0_VAA_VDD2H0	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD
W	CH0_C_RDQS1_T	CH0_C_D11	CH0_C_D10	CH0_C_D8	CH0_D_CK_T1	CH0_D_CA4	CH0_C_CA7	CH0_C_CA6	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS
Y	CH0_C_WCK1_C	VSS	CH0_C_DMI1	VSS	CH0_D_CA2	VSS	CH0_C_CA2	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	AVDD_PLL_DDR1	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD
AA	CH0_C_WCK1_T	CH0_C_D15	CH0_C_D12	CH0_C_D13	CH0_D_CA1	CH0_D_CA3	CH0_C_CKE_CS1	CH0_C_CKE_CS0	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	AVSS_PLL_DDR1	DDR1_REF_CLK	VDD	VSS	VDD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS
AB	CH0_D_D12	VSS	CH0_C_D14	VSS	CH0_D_WCK0_T	VSS	CH0_D_CA0	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	DVDD_PLL_DDR1	VDD_MAC	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AC	CH0_D_WCK1_C	CH0_D_D13	CH0_D_D15	CH0_D_D14	CH0_D_WCK0_C	CH0_D_D6	CH0_D_D7	CH0_D_D5	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	VDD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS
AD	CH0_D_WCK1_T	VSS	CH0_D_DMI1	VSS	CH0_D_RDQS0_T	VSS	CH0_D_D4	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	CH0_VAA_VDD2H1	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD
AE	CH0_D_RDQS1_C	CH0_D_D9	CH0_D_D10	CH0_D_D11	CH0_D_RDQS0_C	CH0_D_D1	CH0_D_D3	CH0_D_DMI0	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	CH0_VDD	AVDD_PLL_DDR2	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AF	CH0_D_RDQS1_T	VSS	CH0_D_D8	VSS	CH0_D_D2	VSS	CH0_D_D0	VSS	CH0_VDD2H	VSS	CH0_VDDQ	VSS	CH0_VDD	VSS	AVSS_PLL_DDR2	DDR2_REF_CLK	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD

Figure 4 Ball Map (Top-Left)

Bottom-Left



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
AG	CH1_A_D2	VSS	CH1_A_D0	VSS	CH1_A_CK_T0	VSS	CH1_A_CA5	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	DVDD_PLL_DDR2	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AH	CH1_A_RDQS0_C	CH1_A_D1	CH1_A_D3	CH1_A_DMI0	CH1_A_CK_C0	CH1_A_CA3	CH1_A_CA4	CH1_A_CA6	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AJ	CH1_A_RDQS0_T	VSS	CH1_A_D4	VSS	CH1_A_CKE_CS0	VSS	CH1_A_CA7	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	CH1_VAA_VDD2H0	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AK	CH1_A_WCK0_C	CH1_A_D6	CH1_A_D5	CH1_A_D7	CH1_A_CKE_CS1	CH1_A_CA2	CH1_B_CA0	CH1_B_CKE_CS0	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AL	CH1_A_WCK0_T	VSS	CH1_A_D8	VSS	CH1_A_CA1	VSS	CH1_B_CA1	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	AVDD_PLL_DDR3	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AM	CH1_A_RDQS1_C	CH1_A_D9	CH1_A_D10	CH1_A_D11	CH1_A_CA0	CH1_AB_PWROK	CH1_B_CA7	CH1_B_CKE_CS1	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	AVSS_PLL_DDR3	DDR3_REF_CLK	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AN	CH1_A_RDQS1_T	VSS	CH1_A_DMI1	VSS	CH1_AB_ATO	VSS	CH1_B_CA2	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	DVDD_PLL_DDR3	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AP	CH1_A_WCK1_C	CH1_A_D13	CH1_A_D12	CH1_A_D14	CH1_B_CK_T1	CH1_AB_ZN	CH1_AB_RESET_N	CH1_B_CA5	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AR	CH1_A_WCK1_T	VSS	CH1_A_D15	VSS	CH1_B_CK_C1	VSS	CH1_AB_DTO	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	CH1_VAA_VDD2H1	VDD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AT	CH1_B_D13	CH1_B_D15	CH1_B_D14	CH1_B_DMI1	CH1_B_D5	CH1_B_CA3	CH1_B_CA6	CH1_B_CA4	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AU	CH1_B_WCK1_C	VSS	CH1_B_D12	VSS	CH1_B_D7	VSS	CH1_B_D2	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	VDD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AV	CH1_B_WCK1_T	CH1_B_D11	CH1_B_D10	CH1_B_D8	CH1_B_D6	CH1_B_DMI0	CH1_B_D1	CH1_B_D0	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
AW	CH1_B_RDQS1_C	VSS	CH1_B_D9	VSS	CH1_B_D4	VSS	CH1_B_D3	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
AY	CH1_B_RDQS1_T	CH1_C_D1	CH1_C_D2	CH1_C_D0	CH1_B_WCK0_T	CH1_B_WCK0_C	CH1_B_RDQS0_T	CH1_B_RDQS0_C	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
BA	CH1_C_RDQS0_C	VSS	CH1_C_D3	VSS	CH1_C_CA5	VSS	CH1_C_CA4	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	EP01_VDDL	VSS	EP01_VDDL	VSS	EP01_VDDL	VSS	EP23_VDDL	VSS	VDD	VSS	VDD	VSS
BB	CH1_C_RDQS0_T	CH1_C_DMI0	CH1_C_D4	CH1_C_D7	CH1_C_CK_C0	CH1_C_CK_T0	CH1_C_CA3	CH1_C_CA0	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	EP01_VPH	VSS	EP01_VPH	VSS	EP23_VDDL	VSS	EP23_VPH	VSS	VDD	VSS	VDD
BC	CH1_C_WCK0_C	VSS	CH1_C_D6	VSS	CH1_C_CKE_CS1	VSS	CH1_C_CKE_CS0	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	EP01_VDDL	VSS	EP01_VDDL	VSS	EP01_VDDL	VSS	EP23_VPH	VSS	VDD	VSS	VDD	VSS
BD	CH1_C_WCK0_T	CH1_C_D5	CH1_C_D9	CH1_C_D8	CH1_C_CA1	CH1_C_CA7	CH1_C_CA2	CH1_C_CA6	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	CH1_VDD	VSS	EP01_VPH	VSS	EP01_VPH	VSS	EP01_VPH	EP_RESREF	VSS	VSS	VDD	VSS	VDD
BE	CH1_C_RDQS1_C	VSS	CH1_C_D10	VSS	CH1_CD_ZN	VSS	CH1_CD_ATO	VSS	CH1_VDD2H	VSS	CH1_VDDQ	VSS	CH1_VDD	VSS	EP01_VDDL	VSS	EP01_VDDL	VSS	EP01_VDDL	VSS	VSS	VSS	VDD	VSS	VDD	VSS
BF	CH1_C_RDQS1_T	CH1_C_D13	CH1_C_D11	CH1_C_DMI1	CH1_CD_PWROK	CH1_CD_DTO	CH1_CD_RESET_N	CH1_D_CKE_CS0	CH1_D_CA0	VSS	VSS	VSS	VSS	VSS	VSS	EP01_VPH	VSS	EP01_VPH	VSS	EP_REF_CLK_M	EP_REF_CLK_P	VSS	VSS	VDD	VSS	VDD
BG	CH1_C_WCK1_C	VSS	CH1_C_D12	VSS	CH1_D_CA1	VSS	CH1_D_CKE_CS1	VSS	CH1_D_CA2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
BH	CH1_C_WCK1_T	CH1_C_D15	CH1_C_D14	CH1_D_D14	CH1_D_CA7	CH1_D_CA3	CH1_D_CK_C1	CH1_D_CA5	CH1_D_CA6	VSS	EP_RX_0_P	VSS	EP_RX_1_P	VSS	EP_RX_2_P	VSS	EP_RX_3_P	VSS	EP_RX_4_P	VSS	EP_RX_5_P	VSS	EP_RX_6_P	VSS	EP_RX_7_P	VSS
BJ	CH1_D_WCK1_C	VSS	CH1_D_D15	VSS	CH1_D_CA4	VSS	CH1_D_CK_T1	VSS	CH1_D_D0	VSS	EP_RX_0_M	VSS	EP_RX_1_M	VSS	EP_RX_2_M	VSS	EP_RX_3_M	VSS	EP_RX_4_M	VSS	EP_RX_5_M	VSS	EP_RX_6_M	VSS	EP_RX_7_M	VSS
BK	CH1_D_WCK1_T	CH1_D_D13	CH1_D_D12	CH1_D_DMI1	CH1_D_D7	CH1_D_D5	CH1_D_DMI0	CH1_D_D3	CH1_D_D2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
BL	CH1_D_D10	VSS	CH1_D_D11	VSS	CH1_D_D6	VSS	CH1_D_D4	VSS	CH1_D_D1	VSS	EP_TX_0_M	VSS	EP_TX_1_M	VSS	EP_TX_2_M	VSS	EP_TX_3_M	VSS	EP_TX_4_M	VSS	EP_TX_5_M	VSS	EP_TX_6_M	VSS	EP_TX_7_M	VSS
BM	VSS	CH1_D_RDQS1_C	CH1_D_RDQS1_T	CH1_D_D9	CH1_D_D8	CH1_D_WCK0_T	CH1_D_WCK0_C	CH1_D_RDQS0_T	CH1_D_RDQS0_C	VSS	EP_TX_0_P	VSS	EP_TX_1_P	VSS	EP_TX_2_P	VSS	EP_TX_3_P	VSS	EP_TX_4_P	VSS	EP_TX_5_P	VSS	EP_TX_6_P	VSS	EP_TX_7_P	VSS

Figure 5 Ball Map (Bottom-Left)

Bottom-Right

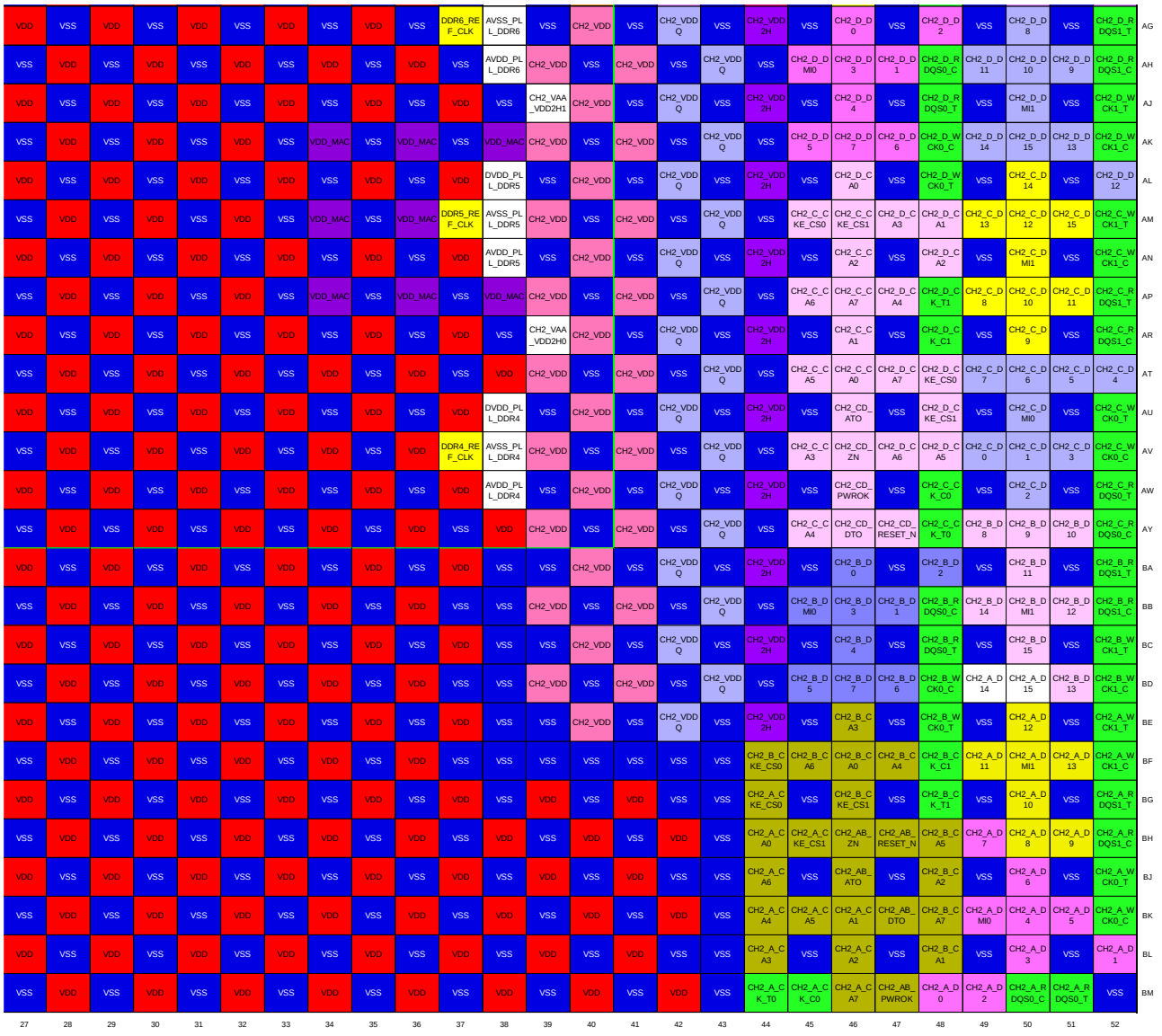
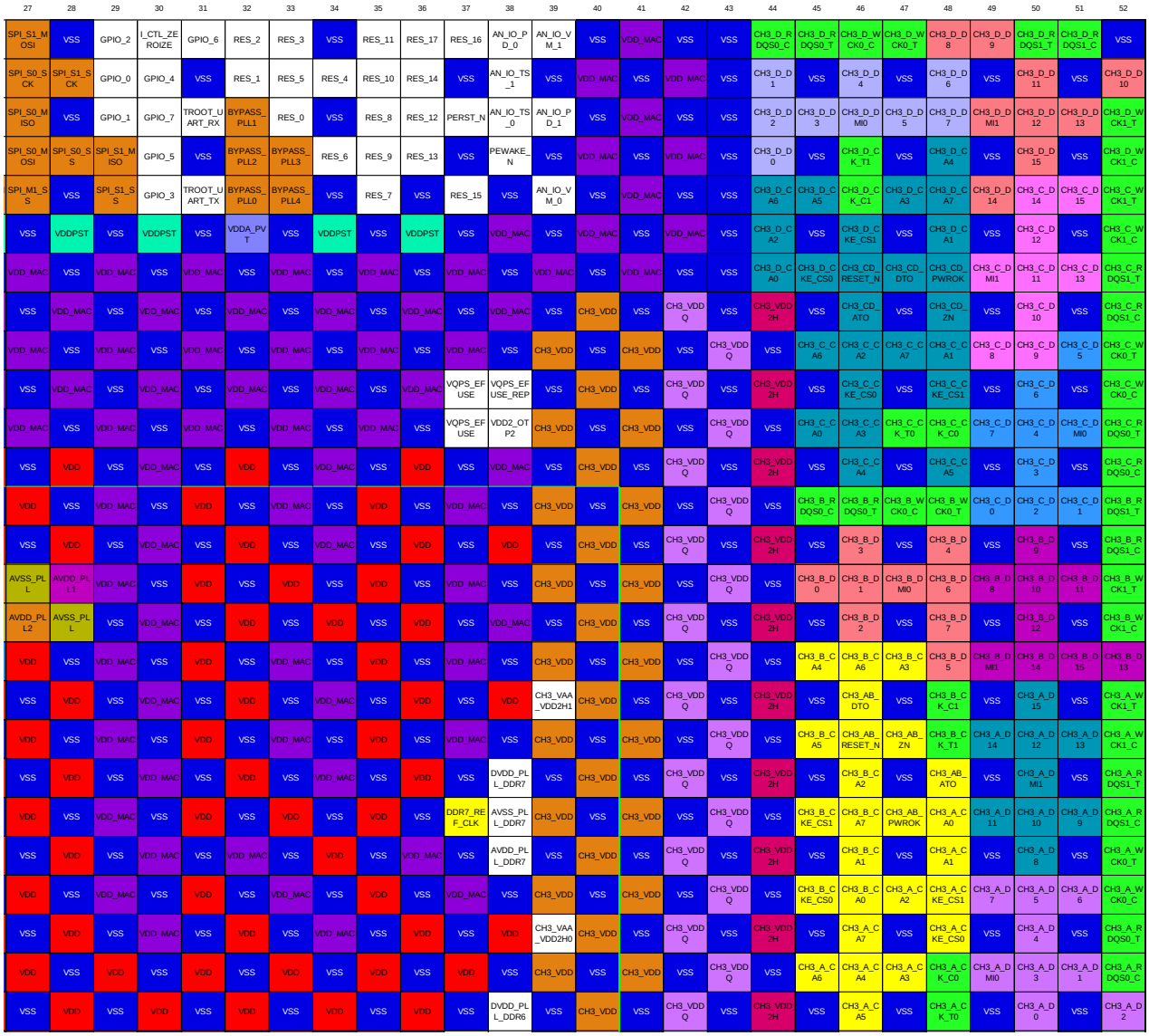


Figure 6 Ball Map (Bottom-Right)

Top-Right



	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	
A	SPI_S1_MOSI	VSS	GPIO_2	I_CTL_ZEROIZE	GPIO_6	RES_2	RES_3	VSS	RES_11	RES_17	RES_16	AN_IO_PD_0	AN_IO_VM_1	VSS	VDD_MAC	VSS	VSS	CH3_D_RDQS0_C	CH3_D_RDQS0_T	CH3_D_WCK0_C	CH3_D_WCK0_T	CH3_D_D8	CH3_D_D9	CH3_D_RDQS1_T	CH3_D_RDQS1_C	VSS	A
B	SPI_S0_SCK	SPI_S1_SCK	GPIO_0	GPIO_4	VSS	RES_1	RES_5	RES_4	RES_10	RES_14	VSS	AN_IO_TS_1	VSS	VDD_MAC	VSS	VDD_MAC	VSS	CH3_D_D1	VSS	CH3_D_D4	VSS	CH3_D_D6	VSS	CH3_D_D11	VSS	CH3_D_D10	B
C	SPI_S0_MISO	VSS	GPIO_1	GPIO_7	TROOT_UART_RX	BYPASS_PLL1	RES_0	VSS	RES_8	RES_12	PERST_N	AN_IO_TS_0	AN_IO_PD_1	VSS	VDD_MAC	VSS	VSS	CH3_D_D2	CH3_D_D3	CH3_D_DMI0	CH3_D_D5	CH3_D_D7	CH3_D_DMI1	CH3_D_D12	CH3_D_D13	CH3_D_WCK1_T	C
D	SPI_S0_MOSI	SPI_S0_SS	SPI_S1_MISO	GPIO_5	VSS	BYPASS_PLL2	BYPASS_PLL3	RES_6	RES_9	RES_13	VSS	PEWAKE_N	VSS	VDD_MAC	VSS	VDD_MAC	VSS	CH3_D_D0	VSS	CH3_D_CK_T1	VSS	CH3_D_CA4	VSS	CH3_D_D15	VSS	CH3_D_WCK1_C	D
E	SPI_M1_SS	VSS	SPI_S1_SS	GPIO_3	TROOT_UART_TX	BYPASS_PLL0	BYPASS_PLL4	VSS	RES_7	VSS	RES_15	VSS	AN_IO_VM_0	VSS	VDD_MAC	VSS	VSS	CH3_D_CA6	CH3_D_CA5	CH3_D_CK_C1	CH3_D_CA3	CH3_D_CA7	CH3_D_D14	CH3_C_D14	CH3_C_D15	CH3_C_WCK1_T	E
F	VSS	VDDPST	VSS	VDDPST	VSS	VDDA_PVT	VSS	VDDPST	VSS	VDDPST	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	CH3_D_CA2	VSS	CH3_D_CKE_CS1	VSS	CH3_D_CA1	VSS	CH3_C_D12	VSS	CH3_C_WCK1_C	F
G	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VSS	CH3_D_CA0	CH3_D_CKE_CS0	CH3_CD_RESET_N	CH3_CD_DTO	CH3_CD_PWROK	CH3_C_DMI1	CH3_C_D11	CH3_C_D13	CH3_C_RDQS1_T	G
H	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_CD_ATO	VSS	CH3_CD_ZN	VSS	CH3_C_D10	VSS	CH3_C_RDQS1_C	H
J	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_C_CA6	CH3_C_CA2	CH3_C_CA7	CH3_C_CA1	CH3_C_D8	CH3_C_D9	CH3_C_D5	CH3_C_WCK0_T	J
K	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VQPS_EFUSE	VQPS_EFUSE_REP	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_C_CKE_CS0	VSS	CH3_C_CKE_CS1	VSS	CH3_C_D6	VSS	CH3_C_WCK0_C	K
L	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VQPS_EFUSE	VDD2_OTP2	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_C_CA0	CH3_C_CA3	CH3_C_CK_T0	CH3_C_CK_C0	CH3_C_D7	CH3_C_D4	CH3_C_DMI0	CH3_C_RDQS0_T	L
M	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_C_CA4	VSS	CH3_C_CA5	VSS	CH3_C_D3	VSS	CH3_C_RDQS0_C	M
N	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_B_RDQS0_C	CH3_B_RDQS0_T	CH3_B_WCK0_C	CH3_B_WCK0_T	CH3_C_D0	CH3_C_D2	CH3_C_D1	CH3_B_RDQS1_T	N
P	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_B_D3	VSS	CH3_B_D4	VSS	CH3_B_D9	VSS	CH3_B_RDQS1_C	P
R	AVSS_PLL	AVDD_PLL1	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_B_D0	CH3_B_D1	CH3_B_DMI0	CH3_B_D6	CH3_B_D8	CH3_B_D10	CH3_B_D11	CH3_B_WCK1_T	R
T	AVDD_PLL2	AVSS_PLL	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_B_D2	VSS	CH3_B_D7	VSS	CH3_B_D12	VSS	CH3_B_WCK1_C	T
U	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_B_CA4	CH3_B_CA6	CH3_B_CA3	CH3_B_D5	CH3_B_DMI1	CH3_B_D14	CH3_B_D15	CH3_B_D13	U
V	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	CH3_VAA_VDD2H1	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_AB_DTO	VSS	CH3_B_CK_C1	VSS	CH3_A_D15	VSS	CH3_A_WCK1_T	V
W	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_B_CA5	CH3_AB_RESET_N	CH3_AB_ZN	CH3_B_CK_T1	CH3_A_D14	CH3_A_D12	CH3_A_D13	CH3_A_WCK1_C	W
Y	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	DVDD_PLL_DDR7	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_B_CA2	VSS	CH3_AB_ATO	VSS	CH3_A_DMI1	VSS	CH3_A_RDQS1_T	Y
AA	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	DDR7_REF_CLK	AVSS_PLL_DDR7	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_B_CKE_CS1	CH3_B_CA7	CH3_AB_PWROK	CH3_A_CA0	CH3_A_D11	CH3_A_D10	CH3_A_D9	CH3_A_RDQS1_C	AA
AB	VSS	VDD	VSS	VDD_MAC	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	AVDD_PLL_DDR7	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_B_CA1	VSS	CH3_A_CA1	VSS	CH3_A_D8	VSS	CH3_A_WCK0_T	AB
AC	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_B_CKE_CS0	CH3_B_CA0	CH3_A_CA2	CH3_A_CKE_CS1	CH3_A_D7	CH3_A_D5	CH3_A_D6	CH3_A_WCK0_C	AC
AD	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD_MAC	VSS	VDD	VSS	VDD	CH3_VAA_VDD2H0	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_A_CA7	VSS	CH3_A_CKE_CS0	VSS	CH3_A_D4	VSS	CH3_A_RDQS0_T	AD
AE	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	CH3_VDD	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_A_CA6	CH3_A_CA4	CH3_A_CA3	CH3_A_CK_C0	CH3_A_DMI0	CH3_A_D3	CH3_A_D1	CH3_A_RDQS0_C	AE
AF	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	DVDD_PLL_DDR6	VSS	CH3_VDD	VSS	CH3_VDDQ	VSS	CH3_VDD2H	VSS	CH3_A_CA5	VSS	CH3_A_CK_T0	VSS	CH3_A_D0	VSS	CH3_A_D2	AF

Figure 7 Ball Map (Top-Right)

3.2 Pin Description

Power and Ground

Table 6 Power and Ground

Name	Type	Description
VDD_MAC	Power	VDD core power for matrix
VDD	Power	VDD core power

AVDD_PLL_DDR[0-7]	Power	PLL analog power for DDR
DVDD_PLL_DDR[0-7]	Power	PLL digital power for DDR
AVDD_PLL1 AVDD_PLL2	Power	PLL analog power for system
CH[0-3]_VAA_VDD2H0 CH[0-3]_VAA_VDD2H1	Power	LPDDR VAA VDD2H (PLL power)
CH[0-3]_VDD	Power	LPDDR VDD (digital power)
CH[0-3]_VDD2H	Power	LPDDR VDD2H (CMOS driver power for CKE)
CH[0-3]_VDDQ	Power	LPDDR VDDQ (IO power)
EP01_VDDL EP23_VDDL	Power	PCIe EP VDDL
EP01_VPH EP23_VPH	Power	PCIe EP VPH
VDDPST	Power	Digital IO power
VDD2_OTP2	Power	OTP power
VQPS_EFUSE VQPS_EFUSE_REP	Power	eFUSE power
VDDA_PVT	Power	Temperature sensor analog power
VSS	Ground	Digital ground
AVSS_PLL	Ground	PLL analog ground for system
AVSS_PLL_DDR[0-7]	Ground	PLL analog ground for DDR

System

Table 7 System

Name	Type	Description
SYS_RST	I	System reset (active low reset)
SYS_POR	I	System power on reset (active low reset)
SYS_REF_CLK	I	System reference clock (50MHz)
DDR[0-7]_REF_CLK	I	DDR reference clock

Testing

Table 8 Testing

Name	Type	Description
BYPASS_PLL[0-4]	I	PLL debug pin
I_CTL_ZEROIZE	I	True random number generator (TRNG) clear signal

DFT_TEST	I	DFT test
TEST	I	System test
MODE_1	I	Test mode 1
MODE_2	I	Test mode 2
AN_IO_PD_[0-1]	B	PVT analog test IO
AN_IO_VM_[0-1]	B	PVT analog test IO
AN_IO_TS_[0-1]	B	PVT analog test IO

PCIe

Table 9 PCIe

Name	Type	Description
EP_RX_[0-7]_P EP_RX_[0-7]_M	I	PCIe differential receive pair[1]
EP_TX_[0-7]_P EP_TX_[0-7]_M	O	PCIe differential transmit pair[2]
EP_REF_CLK_P EP_REF_CLK_M	I	PCIe reference clock signal (100 MHz)
EP_RESREF	B	PCIe EP reference resistor signal
PERST_N	I	PCIe PERST#
PEWAKE_N	B	PCIe PEWAKE#

LPDDR

Table 10 LPDDR

Name	Type	Description
CH[0-3]_[A-D]_CA[0-7]	O	LPDDR command/address signal
CH[0-3]_[A-D]_D[0-15]	B	LPDDR data I/O
CH[0-3]_A_CK_T0 CH[0-3]_B_CK_T1 CH[0-3]_C_CK_T0 CH[0-3]_D_CK_T1	O	LPDDR clock (true)
CH[0-3]_A_CK_C0 CH[0-3]_B_CK_C1 CH[0-3]_C_CK_C0 CH[0-3]_D_CK_C1	O	LPDDR clock (complement)

[1] *PCIe controller and PHY supports 16 RX lanes. N3000 chip only supports 8 lanes in current package.*
[2] *PCIe controller and PHY supports 16 TX lanes. N3000 chip only supports 8 lanes in current package.*

CH[0-3]_[A-D]_CKE_CS[0-1]	O	LPDDR chip select
CH[0-3]_[A-D]_DMI[0-1]	B	LPDDR data mask inversion
CH[0-3]_[A-D]_RDQS[0-1]_T	B	LPDDR read data strobe (true)
CH[0-3]_[A-D]_RDQS[0-1]_C	B	LPDDR read data strobe (complement)
CH[0-3]_[A-D]_WCK[0-1]_T	O	LPDDR data clock (true)
CH[0-3]_[A-D]_WCK[0-1]_C	O	LPDDR data clock (complement)
CH[0-3]_AB_ATO CH[0-3]_CD_ATO	O	LPDDR analog test output
CH[0-3]_AB_DTO CH[0-3]_CD_DTO	O	LPDDR digital test output
CH[0-3]_AB_PWROK CH[0-3]_CD_PWROK	I	LPDDR retention mode control (power good)
CH[0-3]_AB_RESET_N CH[0-3]_CD_RESET_N	O	LPDDR reset
CH[0-3]_AB_ZN CH[0-3]_CD_ZN	I	LPDDR calibration external reference resistor

JTAG

Table 11 JTAG

Name	Type	Description
JTAG_0_TCK	I	JTAG0 (refer to IEEE 1149.1)
JTAG_0_TMS	I	JTAG0 (refer to IEEE 1149.1)
JTAG_0_TDI	I	JTAG0 (refer to IEEE 1149.1)
JTAG_0_TRSTN	I	JTAG0 (refer to IEEE 1149.1)
JTAG_0_TDO	O	JTAG0 (refer to IEEE 1149.1)
JTAG_1_TCK	I	JTAG1 (refer to IEEE 1149.1)
JTAG_1_TMS	I	JTAG1 (refer to IEEE 1149.1)
JTAG_1_TDI	I	JTAG1 (refer to IEEE 1149.1)
JTAG_1_TRSTN	I	JTAG1 (refer to IEEE 1149.1)
JTAG_1_TDO	O	JTAG1 (refer to IEEE 1149.1)

External SPI Debugger

Table 12 Debugger

Name	Type	Description
SPI_DB0_SS	I	QSPI debugger0 chip select
SPI_DB0_SCK	I	QSPI debugger0 clock
SPI_DB0_MOSI	B	QSPI debugger0 data0
SPI_DB0_MISO	B	QSPI debugger0 data1
SPI_DB0_IO2	B	QSPI debugger0 data2
SPI_DB0_IO3	B	QSPI debugger0 data3
SPI_DB1_SS	I	QSPI debugger1 chip select
SPI_DB1_SCK	I	QSPI debugger1 clock
SPI_DB1_MOSI	B	QSPI debugger1 data0
SPI_DB1_MISO	B	QSPI debugger1 data1
SPI_DB1_IO2	B	QSPI debugger1 data2
SPI_DB1_IO3	B	QSPI debugger1 data3

QSPI Flash

Table 13 QSPI

Name	Type	Description
QSPI_SS	O	QSPI Flash chip select
QSPI_SCK	O	QSPI Flash clock
QSPI_MOSI	B	QSPI Flash data0
QSPI_MISO	B	QSPI Flash data1
QSPI_IO2	B	QSPI Flash data2
QSPI_IO3	B	QSPI Flash data3

I^2C

Table 14 I^2C

Name	Type	Description
I2C_SMB_SDA	B	I2C SMBus data (master0)
I2C_SMB_SCL	B	I2C SMBus clock (master0)
I2C_SMB_ALERT	B	I2C SMBus alert (master0)
I2C_M1_SDA	B	I2C data (master1)
I2C_M1_SCL	B	I2C clock (master1)
I2C_S0_SDA	B	I2C data (slave0)
I2C_S0_SCL	B	I2C clock (slave0)
I2C_S1_SDA	B	I2C data (slave1)
I2C_S1_SCL	B	I2C clock (slave1)

SPI

Table 15 SPI

Name	Type	Description
SPI_M0_SS	O	SPI chip select (master 0)
SPI_M0_SCK	O	SPI clock (master 0)
SPI_M0_MOSI	O	SPI output (master 0)
SPI_M0_MISO	I	SPI input (master 0)
SPI_M1_SS	O	SPI chip select (master 1)
SPI_M1_SCK	O	SPI clock (master 1)
SPI_M1_MOSI	O	SPI output (master 1)
SPI_M1_MISO	I	SPI input (master 1)
SPI_S0_SS	I	SPI chip select (slave 0)
SPI_S0_SCK	I	SPI clock (slave 0)
SPI_S0_MOSI	I	SPI output (slave 0)
SPI_S0_MISO	O	SPI input (slave 0)
SPI_S1_SS	I	SPI chip select (slave 1)
SPI_S1_SCK	I	SPI clock (slave 1)
SPI_S1_MOSI	I	SPI output (slave 1)
SPI_S1_MISO	O	SPI input (slave 1)

UART

Table 16 UART

Name	Type	Description
UART0_TX	O	UART0 transmitter signal
UART0_RX	I	UART0 receiver signal
UART1_TX	O	UART1 Transmitter signal
UART1_RX	I	UART1 Receiver signal
TROOT_UART_TX	O	tRoot UART Transmitter signal
TROOT_UART_RX	I	tRoot UART Receiver signal

GPIO

Table 17 GPIO

Name	Type	Description
GPIO_0	I	General purpose IO (Connected to PERST_N)

GPIO_[1-17]	B	General purpose IO
RES_[0-4]	I	Boot option
RES_[5-17]	B	Reserved pin

3.3 Package Skew Data

This table provides package skew data useful for optimizing critical trace layout on the board for high-speed PCIe and LPDDR signals. The data includes the signal's ball number, ball name, length, and flight time.

Table 18 Package Skew Data – PCIe

Ball Name	Ball	Length in Package (um)	Flight Time (ps)
EP_REF_CLK_M	BF20	8992.3079	56.0268
EP_REF_CLK_P	BF21	8961.5601	55.8353
EP_RESREF	BD21	5626.3539	35.0552
EP_RX_0_M	BJ11	9912.6722	61.7612
EP_RX_0_P	BH11	9911.7978	61.7557
EP_RX_1_M	BJ13	9455.2216	58.9110
EP_RX_1_P	BH13	9454.3426	58.9056
EP_RX_2_M	BJ15	8856.4290	55.1802
EP_RX_2_P	BH15	8854.5290	55.1684
EP_RX_3_M	BJ17	9166.0892	57.1096
EP_RX_3_P	BH17	9164.6998	57.1009
EP_RX_4_M	BJ19	9189.2972	57.2542
EP_RX_4_P	BH19	9186.2402	57.2351
EP_RX_5_M	BJ21	9682.1032	60.3246
EP_RX_5_P	BH21	9683.4963	60.3333
EP_RX_6_M	BJ23	11021.1540	68.6676
EP_RX_6_P	BH23	11021.7218	68.6712
EP_RX_7_M	BJ25	11833.3001	73.7277
EP_RX_7_P	BH25	11829.9036	73.7066
EP_TX_0_M	BL11	11364.0992	70.8044
EP_TX_0_P	BM11	11365.7090	70.8144
EP_TX_1_M	BL13	10957.5194	68.2711
EP_TX_1_P	BM13	10958.7312	68.2787
EP_TX_2_M	BL15	10414.4062	64.8873
EP_TX_2_P	BM15	10414.6118	64.8885
EP_TX_3_M	BL17	10637.0438	66.2744

EP_TX_3_P	BM17	10624.6669	66.1973
EP_TX_4_M	BL19	10687.1459	66.5866
EP_TX_4_P	BM19	10688.6502	66.5960
EP_TX_5_M	BL21	11205.2150	69.8144
EP_TX_5_P	BM21	11206.9780	69.8254
EP_TX_6_M	BL23	12564.4049	78.2829
EP_TX_6_P	BM23	12564.9959	78.2866
EP_TX_7_M	BL25	13389.6644	83.4247
EP_TX_7_P	BM25	13391.3758	83.4354

Table 19 Package Skew Data – LPDDR

Ball Name	Ball	Length in Package (um)	Flight Time (ps)
CH0_A_CA0	E9	12711.2212	79.1976
CH0_A_CA1	C7	12958.8527	80.7405
CH0_A_CA2	B7	13700.6619	85.3624
CH0_A_CA3	B9	12636.7316	78.7335
CH0_A_CA4	C9	11875.2121	73.9889
CH0_A_CA5	C8	12177.9849	75.8753
CH0_A_CA6	D9	12706.5923	79.1688
CH0_A_CA7	A7	14407.2199	89.7646
CH0_A_CK_C0	A8	14005.8569	87.2639
CH0_A_CK_T0	A9	14004.0454	87.2526
CH0_A_CKE_CS0	F9	10112.4655	63.0060
CH0_A_CKE_CS1	E8	11251.1683	70.1007
CH0_A_D0	A5	13155.2824	81.9644
CH0_A_D1	B1	15563.1702	96.9668
CH0_A_D10	F3	12322.2784	76.7743
CH0_A_D11	G4	12007.3287	74.8120
CH0_A_D12	H3	12407.2487	77.3037
CH0_A_D13	G2	12970.9598	80.8159
CH0_A_D14	J4	11594.5736	72.2403
CH0_A_D15	J3	12116.1236	75.4899
CH0_A_D2	A4	14195.7700	88.4472
CH0_A_D3	B3	14098.8497	87.8433
CH0_A_D4	C3	13635.1826	84.9544
CH0_A_D5	C2	14496.5846	90.3214
CH0_A_D6	D3	13703.3489	85.3791
CH0_A_D7	E4	12885.3468	80.2825

CH0_A_D8	E3	12493.4451	77.8408
CH0_A_D9	E2	13390.0897	83.4274
CH0_A_DMI0	C4	12761.5090	79.5110
CH0_A_DMI1	G3	12602.2270	78.5185
CH0_A_RDQS0_C	A3	15417.7220	96.0606
CH0_A_RDQS0_T	A2	15413.9798	96.0373
CH0_A_RDQS1_C	E1	14000.8275	87.2326
CH0_A_RDQS1_T	F1	13998.2542	87.2165
CH0_A_WCK0_C	C1	15875.0867	98.9102
CH0_A_WCK0_T	D1	15888.2505	98.9922
CH0_A_WCK1_C	G1	13927.5555	86.7760
CH0_A_WCK1_T	H1	13932.5238	86.8070
CH0_AB_ATO	D7	12688.4319	79.0557
CH0_AB_DTO	C6	13911.9530	86.6788
CH0_AB_PWROK	A6	15089.5409	94.0158
CH0_AB_RESET_N	E6	12677.4479	78.9872
CH0_AB_ZN	E7	12100.2051	75.3907
CH0_B_CA0	G7	12337.6318	76.8700
CH0_B_CA1	B5	15433.6441	96.1598
CH0_B_CA2	D5	14767.4477	92.0090
CH0_B_CA3	H7	11586.4601	72.1898
CH0_B_CA4	G6	12582.1049	78.3932
CH0_B_CA5	E5	13853.4135	86.3141
CH0_B_CA6	G8	11454.2392	71.3660
CH0_B_CA7	C5	14708.3774	91.6410
CH0_B_CK_C1	G5	13580.1348	84.6114
CH0_B_CK_T1	F5	13575.4268	84.5821
CH0_B_CKE_CS0	G9	10462.9252	65.1896
CH0_B_CKE_CS1	F7	12470.3493	77.6969
CH0_B_D0	M7	10904.2166	67.9390
CH0_B_D1	L6	11579.3233	72.1453
CH0_B_D10	N2	10733.5727	66.8758
CH0_B_D11	M3	10807.2234	67.3347
CH0_B_D12	L2	11473.8282	71.4880
CH0_B_D13	J2	11719.4425	73.0183
CH0_B_D14	L4	9836.1427	61.2844
CH0_B_D15	K3	10709.3312	66.7248
CH0_B_D2	M5	12533.3445	78.0894

CH0_B_D3	L7	10664.7330	66.4469
CH0_B_D4	K7	10977.2498	68.3941
CH0_B_D5	J8	10811.7863	67.3632
CH0_B_D6	J6	11552.1780	71.9762
CH0_B_D7	J7	11036.8566	68.7655
CH0_B_D8	N4	9852.0067	61.3832
CH0_B_D9	N3	10228.6085	63.7296
CH0_B_DMI0	L8	9757.5324	60.7946
CH0_B_DMI1	L3	11069.9411	68.9716
CH0_B_RDQS0_C	L5	12612.8206	78.5846
CH0_B_RDQS0_T	K5	12610.9071	78.5726
CH0_B_RDQS1_C	L1	11805.4727	73.5543
CH0_B_RDQS1_T	M1	11805.2933	73.5532
CH0_B_WCK0_C	J5	13107.7456	81.6682
CH0_B_WCK0_T	H5	13114.0060	81.7072
CH0_B_WCK1_C	J1	12963.6412	80.7704
CH0_B_WCK1_T	K1	12958.7609	80.7399
CH0_C_CA0	U7	8464.4730	52.7381
CH0_C_CA1	V7	7360.1049	45.8574
CH0_C_CA2	Y7	5821.2812	36.2697
CH0_C_CA3	R8	8635.9732	53.8067
CH0_C_CA4	N8	10293.3530	64.1330
CH0_C_CA5	U8	7736.8079	48.2044
CH0_C_CA6	W8	6944.5142	43.2680
CH0_C_CA7	W7	6999.9689	43.6135
CH0_C_CK_C0	P5	11856.8366	73.8744
CH0_C_CK_T0	N5	11847.9393	73.8189
CH0_C_CKE_CS0	AA8	4733.4595	29.4920
CH0_C_CKE_CS1	AA7	5762.1695	35.9014
CH0_C_D0	R4	9583.8433	59.7124
CH0_C_D1	R3	9722.0845	60.5737
CH0_C_D10	W3	9253.2861	57.6529
CH0_C_D11	W2	9853.1077	61.3901
CH0_C_D12	AA3	9324.0589	58.0938
CH0_C_D13	AA4	8608.1154	53.6331
CH0_C_D14	AB3	8892.5321	55.4052
CH0_C_D15	AA2	9561.9580	59.5761
CH0_C_D2	P3	10375.1853	64.6429

CH0_C_D3	R2	10280.8616	64.0552
CH0_C_D4	U1	10997.8674	68.5225
CH0_C_D5	U2	10301.0116	64.1808
CH0_C_D6	U3	9719.3810	60.5569
CH0_C_D7	U4	8820.9825	54.9594
CH0_C_D8	W4	8816.8851	54.9339
CH0_C_D9	V3	9713.4046	60.5197
CH0_C_DMI0	T3	9740.9439	60.6912
CH0_C_DMI1	Y3	9717.0424	60.5423
CH0_C_RDQS0_C	N1	12026.4233	74.9310
CH0_C_RDQS0_T	P1	12040.0529	75.0159
CH0_C_RDQS1_C	V1	10830.2881	67.4784
CH0_C_RDQS1_T	W1	10828.3822	67.4666
CH0_C_WCK0_C	R1	11442.5476	71.2931
CH0_C_WCK0_T	T1	11438.1419	71.2657
CH0_C_WCK1_C	Y1	10674.7870	66.5096
CH0_C_WCK1_T	AA1	10669.6187	66.4774
CH0_CD_ATO	T7	9417.5520	58.6763
CH0_CD_DTO	N7	11830.0181	73.7073
CH0_CD_PWROK	P7	10956.4055	68.2642
CH0_CD_RESET_N	N6	11438.1455	71.2657
CH0_CD_ZN	R7	9991.6903	62.2535
CH0_D_CA0	AB7	5729.9895	35.7009
CH0_D_CA1	AA5	7172.0080	44.6854
CH0_D_CA2	Y5	9572.2541	59.6402
CH0_D_CA3	AA6	7513.1436	46.8109
CH0_D_CA4	W6	10976.4394	68.3890
CH0_D_CA5	R5	12233.1607	76.2191
CH0_D_CA6	R6	11059.6480	68.9075
CH0_D_CA7	U6	9095.2743	56.6684
CH0_D_CK_C1	V5	9978.8475	62.1735
CH0_D_CK_T1	W5	9981.1521	62.1879
CH0_D_CKE_CS0	U5	9678.1692	60.3001
CH0_D_CKE_CS1	T5	10422.7545	64.9393
CH0_D_D0	AF7	6569.9538	40.9343
CH0_D_D1	AE6	6715.1745	41.8391
CH0_D_D10	AE3	8134.5233	50.6824
CH0_D_D11	AE4	8063.1525	50.2377

CH0_D_D12	AB1	10370.5386	64.6139
CH0_D_D13	AC2	9279.9439	57.8190
CH0_D_D14	AC4	7937.5208	49.4550
CH0_D_D15	AC3	8387.3213	52.2575
CH0_D_D2	AF5	7342.5686	45.7481
CH0_D_D3	AE7	6175.0649	38.4739
CH0_D_D4	AD7	6177.0275	38.4862
CH0_D_D5	AC8	6508.5885	40.5520
CH0_D_D6	AC6	6597.4919	41.1059
CH0_D_D7	AC7	6679.4952	41.6168
CH0_D_D8	AF3	8395.2559	52.3069
CH0_D_D9	AE2	9004.2538	56.1013
CH0_D_DMI0	AE8	5656.5737	35.2434
CH0_D_DMI1	AD3	8832.2542	55.0296
CH0_D_RDQS0_C	AE5	7532.0132	46.9284
CH0_D_RDQS0_T	AD5	7525.5840	46.8884
CH0_D_RDQS1_C	AE1	9677.0445	60.2931
CH0_D_RDQS1_T	AF1	9679.0758	60.3058
CH0_D_WCK0_C	AC5	8534.3794	53.1737
CH0_D_WCK0_T	AB5	8526.6450	53.1255
CH0_D_WCK1_C	AC1	9992.5702	62.2590
CH0_D_WCK1_T	AD1	10060.2695	62.6808
CH1_A_CA0	AM5	8109.4573	50.5262
CH1_A_CA1	AL5	7259.5730	45.2310
CH1_A_CA2	AK6	7762.9897	48.3675
CH1_A_CA3	AH6	5842.8706	36.4042
CH1_A_CA4	AH7	5906.0004	36.7975
CH1_A_CA5	AG7	5832.9369	36.3423
CH1_A_CA6	AH8	6276.8045	39.1078
CH1_A_CA7	AJ7	5810.9511	36.2053
CH1_A_CK_C0	AH5	7295.9988	45.4579
CH1_A_CK_T0	AG5	7303.6147	45.5054
CH1_A_CKE_CS0	AJ5	6833.4016	42.5757
CH1_A_CKE_CS1	AK5	6905.3265	43.0238
CH1_A_D0	AG3	8451.5576	52.6577
CH1_A_D1	AH2	9058.4477	56.4389
CH1_A_D10	AM3	9505.2380	59.2227
CH1_A_D11	AM4	8793.1651	54.7861

CH1_A_D12	AP3	10107.7200	62.9764
CH1_A_D13	AP2	10572.2416	65.8707
CH1_A_D14	AP4	9536.9703	59.4204
CH1_A_D15	AR3	10249.3439	63.8588
CH1_A_D2	AG1	10035.6744	62.5276
CH1_A_D3	AH3	8424.5411	52.4894
CH1_A_D4	AJ3	8086.6142	50.3839
CH1_A_D5	AK3	8900.2803	55.4535
CH1_A_D6	AK2	9319.8778	58.0678
CH1_A_D7	AK4	7892.0945	49.1719
CH1_A_D8	AL3	9014.8916	56.1675
CH1_A_D9	AM2	10125.3999	63.0866
CH1_A_DMI0	AH4	7390.1006	46.0442
CH1_A_DMI1	AN3	9946.7687	61.9736
CH1_A_RDQS0_C	AH1	10191.2499	63.4969
CH1_A_RDQS0_T	AJ1	10185.3366	63.4600
CH1_A_RDQS1_C	AM1	10797.1592	67.2720
CH1_A_RDQS1_T	AN1	10796.2592	67.2664
CH1_A_WCK0_C	AK1	10814.8572	67.3823
CH1_A_WCK0_T	AL1	10811.1906	67.3594
CH1_A_WCK1_C	AP1	11749.3702	73.2048
CH1_A_WCK1_T	AR1	11748.1360	73.1971
CH1_AB_ATO	AN5	8692.3486	54.1579
CH1_AB_DTO	AR7	9200.1923	57.3221
CH1_AB_PWROK	AM6	7417.8411	46.2171
CH1_AB_RESET_N	AP7	7954.9968	49.5638
CH1_AB_ZN	AP6	8334.9374	51.9311
CH1_B_CA0	AK7	6065.0793	37.7887
CH1_B_CA1	AL7	5123.8547	31.9243
CH1_B_CA2	AN7	5950.0002	37.0717
CH1_B_CA3	AT6	8136.3622	50.6938
CH1_B_CA4	AT8	7471.9845	46.5544
CH1_B_CA5	AP8	6333.7169	39.4624
CH1_B_CA6	AT7	8679.9531	54.0807
CH1_B_CA7	AM7	6159.0128	38.3739
CH1_B_CK_C1	AR5	8313.4248	51.7970
CH1_B_CK_T1	AP5	8322.4397	51.8532
CH1_B_CKE_CS0	AK8	4118.3407	25.6594

CH1_B_CKE_CS1	AM8	5410.8511	33.7125
CH1_B_D0	AV8	7099.9923	44.2367
CH1_B_D1	AV7	7710.2044	48.0387
CH1_B_D10	AV3	10328.7972	64.3539
CH1_B_D11	AV2	11166.5082	69.5733
CH1_B_D12	AU3	10343.6027	64.4461
CH1_B_D13	AT1	11104.6364	69.1878
CH1_B_D14	AT3	10200.1121	63.5521
CH1_B_D15	AT2	10390.3095	64.7371
CH1_B_D2	AU7	7082.3752	44.1269
CH1_B_D3	AW7	8488.0196	52.8849
CH1_B_D4	AW5	9882.9763	61.5762
CH1_B_D5	AT5	8194.6244	51.0568
CH1_B_D6	AV5	9104.5682	56.7263
CH1_B_D7	AU5	8593.0079	53.5390
CH1_B_D8	AV4	9977.3969	62.1645
CH1_B_D9	AW3	10911.7535	67.9860
CH1_B_DMI0	AV6	8613.7827	53.6684
CH1_B_DMI1	AT4	9655.4542	60.1586
CH1_B_RDQS0_C	AY8	10062.1917	62.6928
CH1_B_RDQS0_T	AY7	10062.5206	62.6948
CH1_B_RDQS1_C	AW1	12578.5997	78.3713
CH1_B_RDQS1_T	AY1	12572.4381	78.3329
CH1_B_WCK0_C	AY6	10316.8498	64.2794
CH1_B_WCK0_T	AY5	10317.5900	64.2840
CH1_B_WCK1_C	AU1	11834.9775	73.7382
CH1_B_WCK1_T	AV1	11830.7139	73.7116
CH1_C_CA0	BB8	10073.7129	62.7646
CH1_C_CA1	BD5	11268.3306	70.2077
CH1_C_CA2	BD7	11154.2382	69.4968
CH1_C_CA3	BB7	9782.2457	60.9486
CH1_C_CA4	BA7	10174.4388	63.3921
CH1_C_CA5	BA5	11167.3653	69.5786
CH1_C_CA6	BD8	10632.7138	66.2474
CH1_C_CA7	BD6	10674.0706	66.5051
CH1_C_CK_C0	BB5	11734.2092	73.1103
CH1_C_CK_T0	BB6	11737.1713	73.1288
CH1_C_CKE_CS0	BC7	10469.4048	65.2299

CH1_C_CKE_CS1	BC5	10424.5783	64.9506
CH1_C_D0	AY4	10304.3788	64.2017
CH1_C_D1	AY2	11234.1826	69.9949
CH1_C_D10	BE3	12670.3149	78.9428
CH1_C_D11	BF3	12794.3407	79.7155
CH1_C_D12	BG3	13368.6334	83.2937
CH1_C_D13	BF2	13267.4502	82.6632
CH1_C_D14	BH3	13653.3038	85.0673
CH1_C_D15	BH2	13987.2464	87.1480
CH1_C_D2	AY3	10969.4651	68.3456
CH1_C_D3	BA3	11316.4557	70.5075
CH1_C_D4	BB3	11326.5280	70.5703
CH1_C_D5	BD2	12747.6082	79.4244
CH1_C_D6	BC3	11480.8048	71.5315
CH1_C_D7	BB4	10642.9916	66.3115
CH1_C_D8	BD4	11812.1134	73.5957
CH1_C_D9	BD3	12755.6257	79.4743
CH1_C_DMI0	BB2	11643.3082	72.5440
CH1_C_DMI1	BF4	13139.0855	81.8635
CH1_C_RDQS0_C	BA1	12684.9196	79.0338
CH1_C_RDQS0_T	BB1	12681.6986	79.0137
CH1_C_RDQS1_C	BE1	14299.2401	89.0918
CH1_C_RDQS1_T	BF1	14294.4891	89.0622
CH1_C_WCK0_C	BC1	13659.7968	85.1078
CH1_C_WCK0_T	BD1	13661.5411	85.1186
CH1_C_WCK1_C	BG1	14951.2718	93.1543
CH1_C_WCK1_T	BH1	14945.0440	93.1155
CH1_CD_ATO	BE7	10697.6058	66.6517
CH1_CD_DTO	BF6	11234.4506	69.9966
CH1_CD_PWROK	BF5	11861.5442	73.9037
CH1_CD_RESET_N	BF7	10560.8393	65.7996
CH1_CD_ZN	BE5	11601.6666	72.2845
CH1_D_CA0	BF9	10487.1515	65.3405
CH1_D_CA1	BG5	11975.8403	74.6158
CH1_D_CA2	BG9	10140.0106	63.1776
CH1_D_CA3	BH6	11282.7242	70.2973
CH1_D_CA4	BJ5	13368.6298	83.2936
CH1_D_CA5	BH8	10474.5734	65.2621

CH1_D_CA6	BH9	12059.9544	75.1399
CH1_D_CA7	BH5	12702.2195	79.1416
CH1_D_CK_C1	BH7	13035.3873	81.2174
CH1_D_CK_T1	BJ7	13035.2445	81.2165
CH1_D_CKE_CS0	BF8	10916.3171	68.0144
CH1_D_CKE_CS1	BG7	11899.9831	74.1432
CH1_D_D0	BJ9	9838.0242	61.2961
CH1_D_D1	BL9	11323.8057	70.5533
CH1_D_D10	BL1	16172.7271	100.7647
CH1_D_D11	BL3	15011.6612	93.5306
CH1_D_D12	BK3	14900.2708	92.8366
CH1_D_D13	BK2	14935.9542	93.0589
CH1_D_D14	BH4	13876.6233	86.4587
CH1_D_D15	BJ3	14439.7571	89.9673
CH1_D_D2	BK9	10664.5831	66.4460
CH1_D_D3	BK8	10241.7369	63.8114
CH1_D_D4	BL7	12732.4045	79.3296
CH1_D_D5	BK6	12756.9368	79.4825
CH1_D_D6	BL5	13396.8589	83.4695
CH1_D_D7	BK5	13386.3995	83.4044
CH1_D_D8	BM5	14126.8095	88.0175
CH1_D_D9	BM4	14649.6252	91.2749
CH1_D_DMI0	BK7	11592.1024	72.2249
CH1_D_DMI1	BK4	14457.2543	90.0764
CH1_D_RDQS0_C	BM9	12792.8930	79.7065
CH1_D_RDQS0_T	BM8	12784.0876	79.6516
CH1_D_RDQS1_C	BM2	15705.2195	97.8518
CH1_D_RDQS1_T	BM3	15724.7309	97.9734
CH1_D_WCK0_C	BM7	13549.4305	84.4201
CH1_D_WCK0_T	BM6	13545.9915	84.3987
CH1_D_WCK1_C	BJ1	16506.1217	102.8419
CH1_D_WCK1_T	BK1	16508.4311	102.8563
CH2_A_CA0	BH44	12711.2212	79.1976
CH2_A_CA1	BK46	12958.8527	80.7405
CH2_A_CA2	BL46	13700.6619	85.3624
CH2_A_CA3	BL44	12636.7316	78.7335
CH2_A_CA4	BK44	11875.2121	73.9889
CH2_A_CA5	BK45	12177.9849	75.8753

CH2_A_CA6	BJ44	12706.5923	79.1688
CH2_A_CA7	BM46	14407.2199	89.7646
CH2_A_CK_C0	BM45	14005.8569	87.2639
CH2_A_CK_T0	BM44	14004.0454	87.2526
CH2_A_CKE_CS0	BG44	10112.4655	63.0060
CH2_A_CKE_CS1	BH45	11251.1683	70.1007
CH2_A_D0	BM48	13155.2836	81.9644
CH2_A_D1	BL52	15563.1702	96.9668
CH2_A_D10	BG50	12322.2784	76.7743
CH2_A_D11	BF49	11983.1357	74.6613
CH2_A_D12	BE50	12407.2487	77.3037
CH2_A_D13	BF51	12970.9598	80.8159
CH2_A_D14	BD49	11594.5736	72.2403
CH2_A_D15	BD50	12116.1236	75.4899
CH2_A_D2	BM49	14195.7700	88.4472
CH2_A_D3	BL50	14103.8040	87.8742
CH2_A_D4	BK50	13639.5733	84.9818
CH2_A_D5	BK51	14496.5846	90.3214
CH2_A_D6	BJ50	13703.3489	85.3791
CH2_A_D7	BH49	12885.3468	80.2825
CH2_A_D8	BH50	12493.4451	77.8408
CH2_A_D9	BH51	13390.0897	83.4274
CH2_A_DMI0	BK49	12748.1691	79.4278
CH2_A_DMI1	BF50	12602.2270	78.5185
CH2_A_RDQS0_C	BM50	15417.7220	96.0606
CH2_A_RDQS0_T	BM51	15416.4651	96.0527
CH2_A_RDQS1_C	BH52	14000.8275	87.2326
CH2_A_RDQS1_T	BG52	13998.2542	87.2165
CH2_A_WCK0_C	BK52	15875.0867	98.9102
CH2_A_WCK0_T	BJ52	15888.2505	98.9922
CH2_A_WCK1_C	BF52	13927.5555	86.7760
CH2_A_WCK1_T	BE52	13932.5238	86.8070
CH2_AB_ATO	BJ46	12688.4319	79.0557
CH2_AB_DTO	BK47	13911.9530	86.6788
CH2_AB_PWROK	BM47	15089.5409	94.0158
CH2_AB_RESET_N	BH47	12677.4479	78.9872
CH2_AB_ZN	BH46	12100.2051	75.3907
CH2_B_CA0	BF46	12337.6318	76.8700

CH2_B_CA1	BL48	15433.6441	96.1598
CH2_B_CA2	BJ48	14782.7133	92.1041
CH2_B_CA3	BE46	11598.7968	72.2666
CH2_B_CA4	BF47	12597.3705	78.4883
CH2_B_CA5	BH48	13865.7501	86.3910
CH2_B_CA6	BF45	11454.2392	71.3660
CH2_B_CA7	BK48	14708.3774	91.6410
CH2_B_CK_C1	BF48	13586.9709	84.6540
CH2_B_CK_T1	BG48	13582.2630	84.6247
CH2_B_CKE_CS0	BF44	10462.9252	65.1896
CH2_B_CKE_CS1	BG46	12470.3493	77.6969
CH2_B_D0	BA46	10904.2166	67.9390
CH2_B_D1	BB47	11579.3233	72.1453
CH2_B_D10	AY51	10733.5727	66.8758
CH2_B_D11	BA50	10807.2234	67.3347
CH2_B_D12	BB51	11473.8282	71.4880
CH2_B_D13	BD51	11719.4425	73.0183
CH2_B_D14	BB49	9836.1427	61.2844
CH2_B_D15	BC50	10709.3312	66.7248
CH2_B_D2	BA48	12533.3445	78.0894
CH2_B_D3	BB46	10664.7330	66.4469
CH2_B_D4	BC46	10986.8450	68.4539
CH2_B_D5	BD45	10831.5286	67.4862
CH2_B_D6	BD47	11560.9648	72.0309
CH2_B_D7	BD46	11045.6434	68.8202
CH2_B_D8	AY49	9852.0067	61.3832
CH2_B_D9	AY50	10228.6085	63.7296
CH2_B_DMI0	BB45	9757.5324	60.7946
CH2_B_DMI1	BB50	11069.9411	68.9716
CH2_B_RDQS0_C	BB48	12612.8206	78.5846
CH2_B_RDQS0_T	BC48	12609.6645	78.5649
CH2_B_RDQS1_C	BB52	11805.4727	73.5543
CH2_B_RDQS1_T	BA52	11805.2933	73.5532
CH2_B_WCK0_C	BD48	13107.7456	81.6682
CH2_B_WCK0_T	BE48	13114.0060	81.7072
CH2_B_WCK1_C	BD52	12963.6412	80.7704
CH2_B_WCK1_T	BC52	12958.7609	80.7399
CH2_C_CA0	AT46	8464.4730	52.7381

CH2_C_CA1	AR46	7360.1049	45.8574
CH2_C_CA2	AN46	5821.2812	36.2697
CH2_C_CA3	AV45	8635.9732	53.8067
CH2_C_CA4	AY45	10293.3530	64.1330
CH2_C_CA5	AT45	7736.8079	48.2044
CH2_C_CA6	AP45	6944.5142	43.2680
CH2_C_CA7	AP46	6999.9689	43.6135
CH2_C_CK_C0	AW48	11856.8366	73.8744
CH2_C_CK_T0	AY48	11847.9393	73.8189
CH2_C_CKE_CS0	AM45	4732.6765	29.4871
CH2_C_CKE_CS1	AM46	5762.1695	35.9014
CH2_C_D0	AV49	9583.8433	59.7124
CH2_C_D1	AV50	9722.0845	60.5737
CH2_C_D10	AP50	9253.2861	57.6529
CH2_C_D11	AP51	9853.1077	61.3901
CH2_C_D12	AM50	9324.0589	58.0938
CH2_C_D13	AM49	8608.1154	53.6331
CH2_C_D14	AL50	8892.5321	55.4052
CH2_C_D15	AM51	9561.9580	59.5761
CH2_C_D2	AW50	10375.1853	64.6429
CH2_C_D3	AV51	10279.0712	64.0441
CH2_C_D4	AT52	10997.8674	68.5225
CH2_C_D5	AT51	10301.0116	64.1808
CH2_C_D6	AT50	9719.3810	60.5569
CH2_C_D7	AT49	8820.9825	54.9594
CH2_C_D8	AP49	8816.8851	54.9339
CH2_C_D9	AR50	9713.4046	60.5197
CH2_C_DMI0	AU50	9740.9439	60.6912
CH2_C_DMI1	AN50	9717.0424	60.5423
CH2_C_RDQS0_C	AY52	12026.4233	74.9310
CH2_C_RDQS0_T	AW52	12040.0529	75.0159
CH2_C_RDQS1_C	AR52	10830.2881	67.4784
CH2_C_RDQS1_T	AP52	10828.3822	67.4666
CH2_C_WCK0_C	AV52	11442.5476	71.2931
CH2_C_WCK0_T	AU52	11438.1419	71.2657
CH2_C_WCK1_C	AN52	10674.7870	66.5096
CH2_C_WCK1_T	AM52	10669.6187	66.4774
CH2_CD_ATO	AU46	9417.5520	58.6763

CH2_CD_DTO	AY46	11830.0181	73.7073
CH2_CD_PWROK	AW46	10956.4055	68.2642
CH2_CD_RESET_N	AY47	11438.1455	71.2657
CH2_CD_ZN	AV46	9991.6903	62.2535
CH2_D_CA0	AL46	5729.9895	35.7009
CH2_D_CA1	AM48	7166.4935	44.6510
CH2_D_CA2	AN48	9563.1165	59.5833
CH2_D_CA3	AM47	7513.1436	46.8109
CH2_D_CA4	AP47	10964.3112	68.3135
CH2_D_CA5	AV48	12233.1607	76.2191
CH2_D_CA6	AV47	11059.6480	68.9075
CH2_D_CA7	AT47	9095.2743	56.6684
CH2_D_CK_C1	AR48	9978.9995	62.1745
CH2_D_CK_T1	AP48	9981.3144	62.1889
CH2_D_CKE_CS0	AT48	9678.1692	60.3001
CH2_D_CKE_CS1	AU48	10422.7545	64.9393
CH2_D_D0	AG46	6569.9538	40.9343
CH2_D_D1	AH47	6714.2431	41.8333
CH2_D_D10	AH50	8134.5233	50.6824
CH2_D_D11	AH49	8063.1525	50.2377
CH2_D_D12	AL52	10370.5386	64.6139
CH2_D_D13	AK51	9279.9439	57.8190
CH2_D_D14	AK49	7937.5208	49.4550
CH2_D_D15	AK50	8387.3213	52.2575
CH2_D_D2	AG48	7342.5686	45.7481
CH2_D_D3	AH46	6138.1140	38.2437
CH2_D_D4	AJ46	6177.0275	38.4862
CH2_D_D5	AK45	6555.9954	40.8473
CH2_D_D6	AK47	6684.4748	41.6478
CH2_D_D7	AK46	6679.4952	41.6168
CH2_D_D8	AG50	8395.2559	52.3069
CH2_D_D9	AH51	9004.2538	56.1013
CH2_D_DMI0	AH45	5637.7032	35.1259
CH2_D_DMI1	AJ50	8832.2542	55.0296
CH2_D_RDQS0_C	AH48	7532.0132	46.9284
CH2_D_RDQS0_T	AJ48	7525.5840	46.8884
CH2_D_RDQS1_C	AH52	9677.0445	60.2931
CH2_D_RDQS1_T	AG52	9679.0758	60.3058

CH2_D_WCK0_C	AK48	8534.3794	53.1737
CH2_D_WCK0_T	AL48	8526.6450	53.1255
CH2_D_WCK1_C	AK52	9992.5702	62.2590
CH2_D_WCK1_T	AJ52	10060.2695	62.6808
CH3_A_CA0	AA48	8109.4573	50.5262
CH3_A_CA1	AB48	7259.5730	45.2310
CH3_A_CA2	AC47	7762.9897	48.3675
CH3_A_CA3	AE47	5842.8706	36.4042
CH3_A_CA4	AE46	5906.0004	36.7975
CH3_A_CA5	AF46	5832.9369	36.3423
CH3_A_CA6	AE45	6276.8045	39.1078
CH3_A_CA7	AD46	5810.9511	36.2053
CH3_A_CK_C0	AE48	7295.9988	45.4579
CH3_A_CK_T0	AF48	7303.6147	45.5054
CH3_A_CKE_CS0	AD48	6833.4016	42.5757
CH3_A_CKE_CS1	AC48	6905.3265	43.0238
CH3_A_D0	AF50	8451.5576	52.6577
CH3_A_D1	AE51	9058.4477	56.4389
CH3_A_D10	AA50	9505.2380	59.2227
CH3_A_D11	AA49	8793.1651	54.7861
CH3_A_D12	W50	10107.7200	62.9764
CH3_A_D13	W51	10572.2416	65.8707
CH3_A_D14	W49	9536.9703	59.4204
CH3_A_D15	V50	10249.3439	63.8588
CH3_A_D2	AF52	10035.6744	62.5276
CH3_A_D3	AE50	8424.5411	52.4894
CH3_A_D4	AD50	8110.7132	50.5340
CH3_A_D5	AC50	8900.2803	55.4535
CH3_A_D6	AC51	9319.8778	58.0678
CH3_A_D7	AC49	7892.0945	49.1719
CH3_A_D8	AB50	9014.8916	56.1675
CH3_A_D9	AA51	10125.3999	63.0866
CH3_A_DMI0	AE49	7414.1995	46.1944
CH3_A_DMI1	Y50	9946.7687	61.9736
CH3_A_RDQS0_C	AE52	10191.2499	63.4969
CH3_A_RDQS0_T	AD52	10185.3366	63.4600
CH3_A_RDQS1_C	AA52	10797.1592	67.2720
CH3_A_RDQS1_T	Y52	10796.2592	67.2664

CH3_A_WCK0_C	AC52	10814.8572	67.3823
CH3_A_WCK0_T	AB52	10811.1906	67.3594
CH3_A_WCK1_C	W52	11749.3702	73.2048
CH3_A_WCK1_T	V52	11748.1360	73.1971
CH3_AB_ATO	Y48	8692.3486	54.1579
CH3_AB_DTO	V46	9200.1923	57.3221
CH3_AB_PWROK	AA47	7417.8411	46.2171
CH3_AB_RESET_N	W46	7954.9968	49.5638
CH3_AB_ZN	W47	8334.9374	51.9311
CH3_B_CA0	AC46	6065.0793	37.7887
CH3_B_CA1	AB46	5123.8547	31.9243
CH3_B_CA2	Y46	5950.0002	37.0717
CH3_B_CA3	U47	8136.3622	50.6938
CH3_B_CA4	U45	7470.5680	46.5456
CH3_B_CA5	W45	6333.7169	39.4624
CH3_B_CA6	U46	8680.6757	54.0852
CH3_B_CA7	AA46	6159.0128	38.3739
CH3_B_CK_C1	V48	8313.4248	51.7970
CH3_B_CK_T1	W48	8322.4397	51.8532
CH3_B_CKE_CS0	AC45	4118.1815	25.6585
CH3_B_CKE_CS1	AA45	5410.8511	33.7125
CH3_B_D0	R45	7099.9923	44.2367
CH3_B_D1	R46	7710.2044	48.0387
CH3_B_D10	R50	10328.7972	64.3539
CH3_B_D11	R51	11166.5082	69.5733
CH3_B_D12	T50	10343.6027	64.4461
CH3_B_D13	U52	11095.6936	69.1320
CH3_B_D14	U50	10200.1121	63.5521
CH3_B_D15	U51	10390.3095	64.7371
CH3_B_D2	T46	7082.3752	44.1269
CH3_B_D3	P46	8488.0196	52.8849
CH3_B_D4	P48	9864.5608	61.4614
CH3_B_D5	U48	8194.6244	51.0568
CH3_B_D6	R48	9093.7152	56.6587
CH3_B_D7	T48	8593.0079	53.5390
CH3_B_D8	R49	9977.3969	62.1645
CH3_B_D9	P50	10911.7535	67.9860
CH3_B_DMI0	R47	8613.7827	53.6684

CH3_B_DMI1	U49	9655.4542	60.1586
CH3_B_RDQS0_C	N45	10062.1917	62.6928
CH3_B_RDQS0_T	N46	10062.5206	62.6948
CH3_B_RDQS1_C	P52	12578.5997	78.3713
CH3_B_RDQS1_T	N52	12572.4381	78.3329
CH3_B_WCK0_C	N47	10315.6841	64.2722
CH3_B_WCK0_T	N48	10316.8050	64.2792
CH3_B_WCK1_C	T52	11834.9775	73.7382
CH3_B_WCK1_T	R52	11830.7139	73.7116
CH3_C_CA0	L45	10074.4071	62.7689
CH3_C_CA1	J48	11268.3306	70.2077
CH3_C_CA2	J46	11154.2382	69.4968
CH3_C_CA3	L46	9782.2457	60.9486
CH3_C_CA4	M46	10174.4388	63.3921
CH3_C_CA5	M48	11167.3653	69.5786
CH3_C_CA6	J45	10632.7138	66.2474
CH3_C_CA7	J47	10674.0706	66.5051
CH3_C_CK_C0	L48	11734.2092	73.1103
CH3_C_CK_T0	L47	11737.1713	73.1288
CH3_C_CKE_CS0	K46	10469.4048	65.2299
CH3_C_CKE_CS1	K48	10424.5783	64.9506
CH3_C_D0	N49	10304.3788	64.2017
CH3_C_D1	N51	11234.1826	69.9949
CH3_C_D10	H50	12670.3149	78.9428
CH3_C_D11	G50	12794.3407	79.7155
CH3_C_D12	F50	13368.6334	83.2937
CH3_C_D13	G51	13267.4502	82.6632
CH3_C_D14	E50	13653.2921	85.0672
CH3_C_D15	E51	13987.2464	87.1480
CH3_C_D2	N50	10969.4651	68.3456
CH3_C_D3	M50	11316.4557	70.5075
CH3_C_D4	L50	11326.5280	70.5703
CH3_C_D5	J51	12747.6082	79.4244
CH3_C_D6	K50	11480.8048	71.5315
CH3_C_D7	L49	10642.9916	66.3115
CH3_C_D8	J49	11812.1134	73.5957
CH3_C_D9	J50	12755.6257	79.4743
CH3_C_DMI0	L51	11643.3082	72.5440

CH3_C_DMI1	G49	13139.0855	81.8635
CH3_C_RDQS0_C	M52	12684.9196	79.0338
CH3_C_RDQS0_T	L52	12681.6986	79.0137
CH3_C_RDQS1_C	H52	14299.2401	89.0918
CH3_C_RDQS1_T	G52	14294.4891	89.0622
CH3_C_WCK0_C	K52	13659.7968	85.1078
CH3_C_WCK0_T	J52	13661.5411	85.1186
CH3_C_WCK1_C	F52	14951.2718	93.1543
CH3_C_WCK1_T	E52	14945.0440	93.1155
CH3_CD_ATO	H46	10697.6058	66.6517
CH3_CD_DTO	G47	11234.4506	69.9966
CH3_CD_PWROK	G48	11861.5442	73.9037
CH3_CD_RESET_N	G46	10560.8393	65.7996
CH3_CD_ZN	H48	11601.6666	72.2845
CH3_D_CA0	G44	10496.3355	65.3977
CH3_D_CA1	F48	11975.8403	74.6158
CH3_D_CA2	F44	10140.0106	63.1776
CH3_D_CA3	E47	11282.7242	70.2973
CH3_D_CA4	D48	13368.6298	83.2936
CH3_D_CA5	E45	10474.5734	65.2621
CH3_D_CA6	E44	12090.6060	75.3309
CH3_D_CA7	E48	12702.2195	79.1416
CH3_D_CK_C1	E46	13035.3873	81.2174
CH3_D_CK_T1	D46	13035.2445	81.2165
CH3_D_CKE_CS0	G45	10916.3171	68.0144
CH3_D_CKE_CS1	F46	11899.9831	74.1432
CH3_D_D0	D44	9838.0242	61.2961
CH3_D_D1	B44	11323.8057	70.5533
CH3_D_D10	B52	16172.7271	100.7647
CH3_D_D11	B50	15011.6612	93.5306
CH3_D_D12	C50	14900.2708	92.8366
CH3_D_D13	C51	14935.9542	93.0589
CH3_D_D14	E49	13876.6233	86.4587
CH3_D_D15	D50	14439.7571	89.9673
CH3_D_D2	C44	10664.5831	66.4460
CH3_D_D3	C45	10241.7369	63.8114
CH3_D_D4	B46	12736.4281	79.3547
CH3_D_D5	C47	12756.9368	79.4825

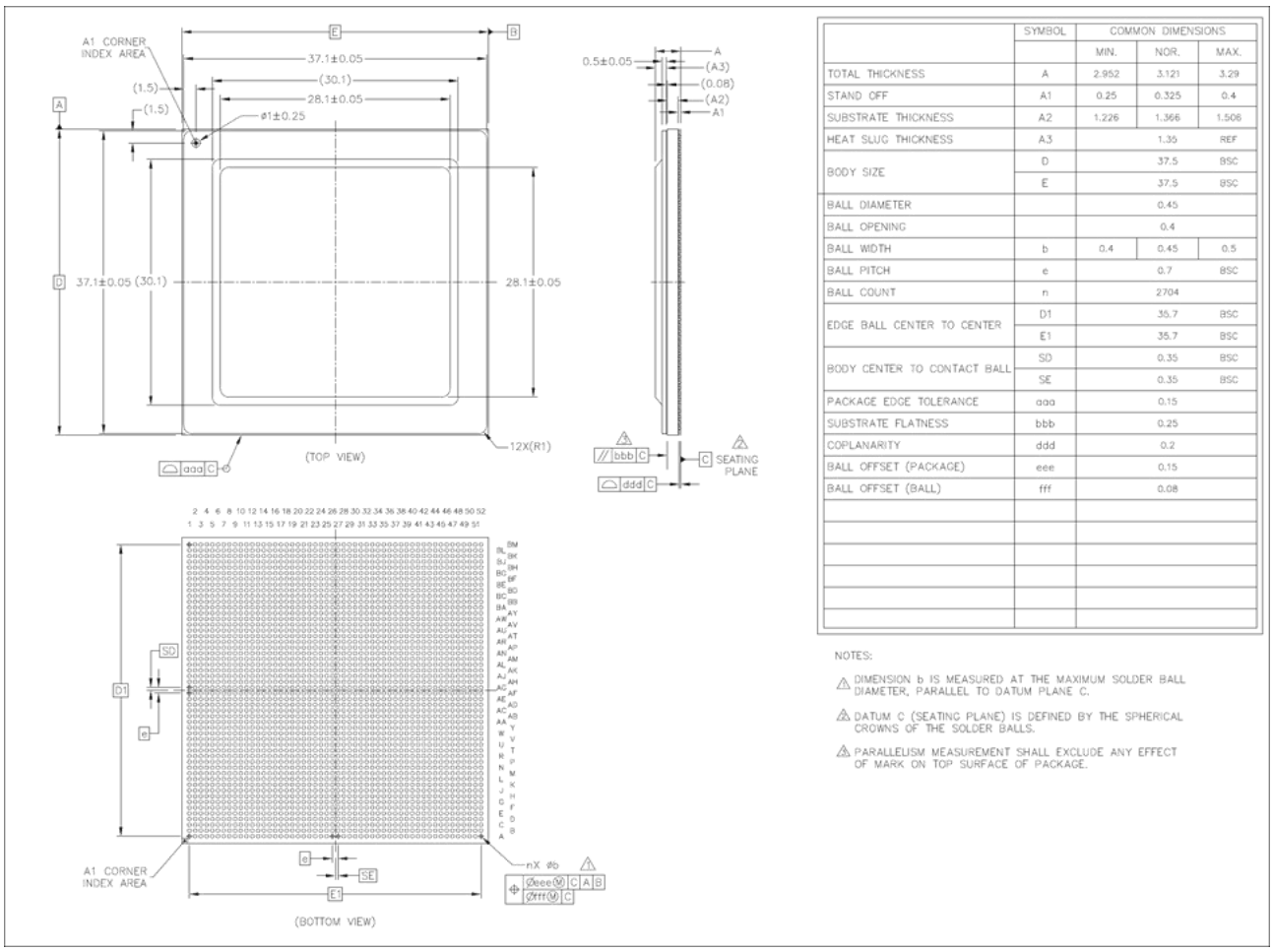
CH3_D_D6	B48	13396.8589	83.4695
CH3_D_D7	C48	13386.3995	83.4044
CH3_D_D8	A48	14126.8095	88.0175
CH3_D_D9	A49	14649.6252	91.2749
CH3_D_DMI0	C46	11592.3601	72.2265
CH3_D_DMI1	C49	14457.2543	90.0764
CH3_D_RDQS0_C	A44	12792.8930	79.7065
CH3_D_RDQS0_T	A45	12785.7294	79.6619
CH3_D_RDQS1_C	A51	15705.2195	97.8518
CH3_D_RDQS1_T	A50	15724.7309	97.9734
CH3_D_WCK0_C	A46	13549.4305	84.4201
CH3_D_WCK0_T	A47	13545.9915	84.3987
CH3_D_WCK1_C	D52	16506.1217	102.8419
CH3_D_WCK1_T	C52	16508.4311	102.8563
DDR0_REF_CLK	R16	1605.9823	10.0061
DDR1_REF_CLK	AA16	1714.8356	10.6843
DDR2_REF_CLK	AF16	1447.8405	9.0208
DDR3_REF_CLK	AM16	2043.4171	12.7316
DDR4_REF_CLK	AV37	1620.9482	10.0994
DDR5_REF_CLK	AM37	2038.8244	12.7030
DDR6_REF_CLK	AG37	1595.8123	9.9428
DDR7_REF_CLK	AA37	1331.2811	8.2946

Table 20 Package Skew Data – QSPI

Ball Name	Ball	Length in Package (um)	Flight Time (ps)
QSPI_SS	B17	10091.6747	71.9293
QSPI_SCK	A17	10768.4788	76.7532
QSPI_MOSI	B15	10347.4373	73.7522
QSPI_MISO	A15	10869.3013	77.4719
QSPI_IO2	B16	10288.0463	73.3289
QSPI_IO3	D16	8741.9867	62.3092

4 Package Information

Raptor is in 37.5 mm x 37.5 mm package with 0.7-mm ball pitch.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	2.952	3.121	3.29
STAND OFF	A1	0.25	0.325	0.4
SUBSTRATE THICKNESS	A2	1.226	1.366	1.506
HEAT SLUG THICKNESS	A3		1.35	REF
BODY SIZE	D		37.5	BSC
	E		37.5	BSC
BALL DIAMETER			0.45	
BALL OPENING			0.4	
BALL WIDTH	b	0.4	0.45	0.5
BALL PITCH	e		0.7	BSC
BALL COUNT	n		2704	
EDGE BALL CENTER TO CENTER	D1		35.7	BSC
	E1		35.7	BSC
BODY CENTER TO CONTACT BALL	SD		0.35	BSC
	SE		0.35	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
SUBSTRATE FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 8 2704-Ball HFCBGA – 37.5mm x 37.5mm x 3.27mm

5 Power Sequence

5.1 Power-On Sequence

SYS_POR releases Raptor chip from reset status. For this to occur, chip operating parameters must meet conditions:

- Chip power rails must be stable and at full voltage for at least 300 ns (t_{POR})
- SYS_REF_CLK inputs must be stable before SYS_POR releases.
- The ramp time for DVDD_PLL_DDR* is between 10 to 200 us (t_1)
- The ramp time for AVDD_PLL_DDR* and VQPS_EFUSE is between 30 to 200 us (t_2)

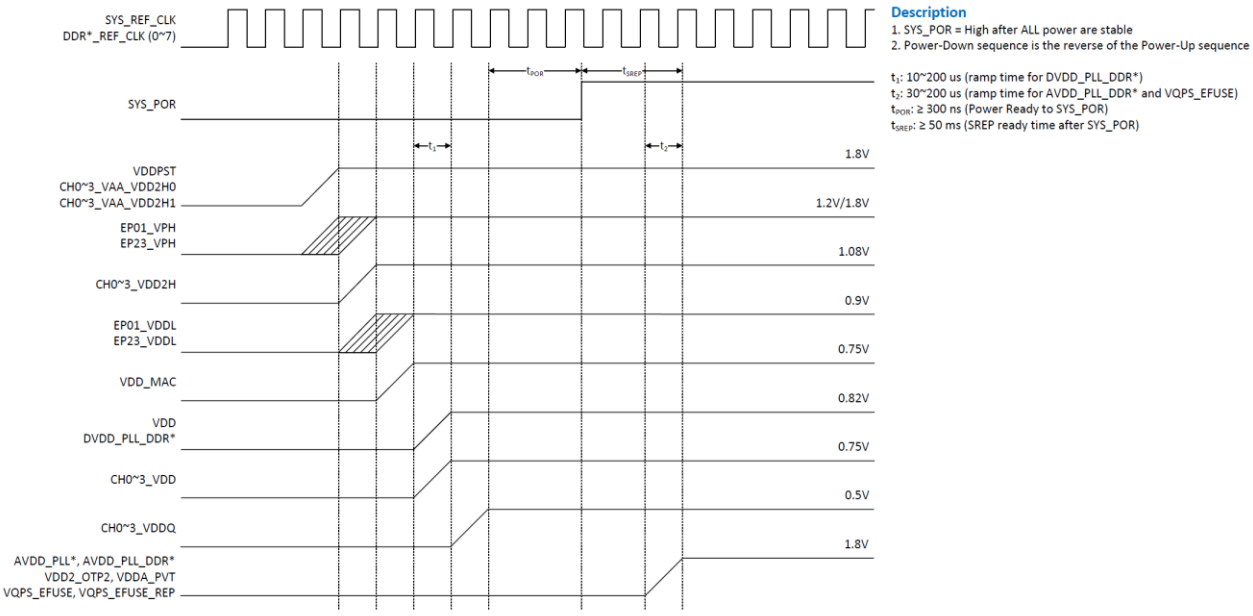


Figure 9 Power-On Sequence

5.2 Power-Down Sequence

Power down sequence is the reverse of the power on sequence.

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